

L-A780 Ver:0.2 (MS-7389L2 Ver:0B)

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CPU:

AMD AM2+
AMD AMD Athlon 64 X2
AMD Athlon 64 FX
AMD Athlon 64
AMD Sempron CPUs

System Chipset:

AMD - RS780 (North Bridge)
- RX780 (North Bridge)
AMD - SB700 (South Bridge)

On Board Chipset:

BIOS - SPI
Azalia CODEC - Realtek ALC662(Default)/888
LPC Super I/O -- ITE IT8718F(GX)
LAN - Marvell 8039/8056/8071/8075/8070(Default)
IEEE1394 - VIA VT6308P
TMP - WPCT200(Default)/ST19WP18
Asset ID - PCA24S08
HWM W83201G

Main Memory:

DDR II * 4 (Max 4GB)

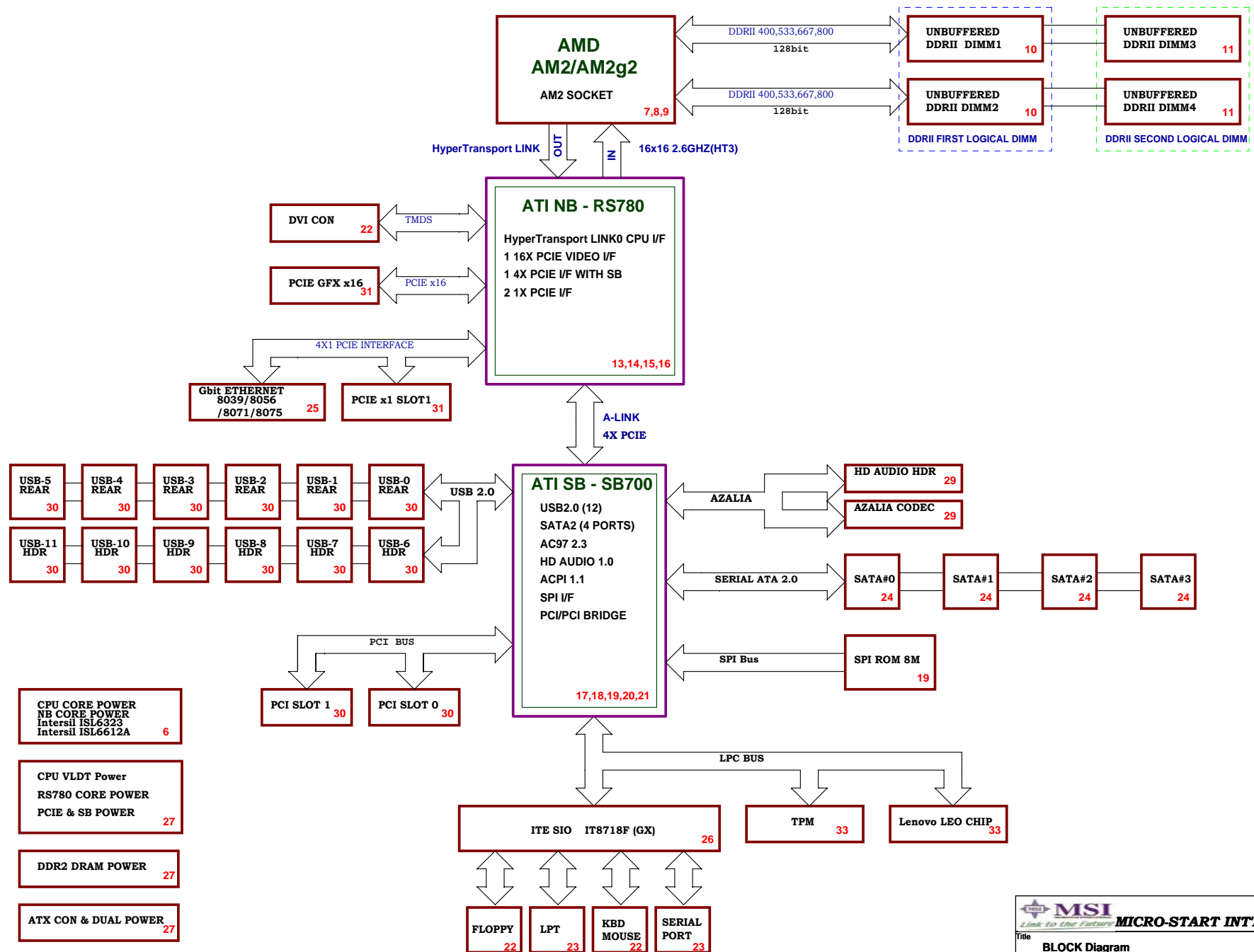
Expansion Slots:

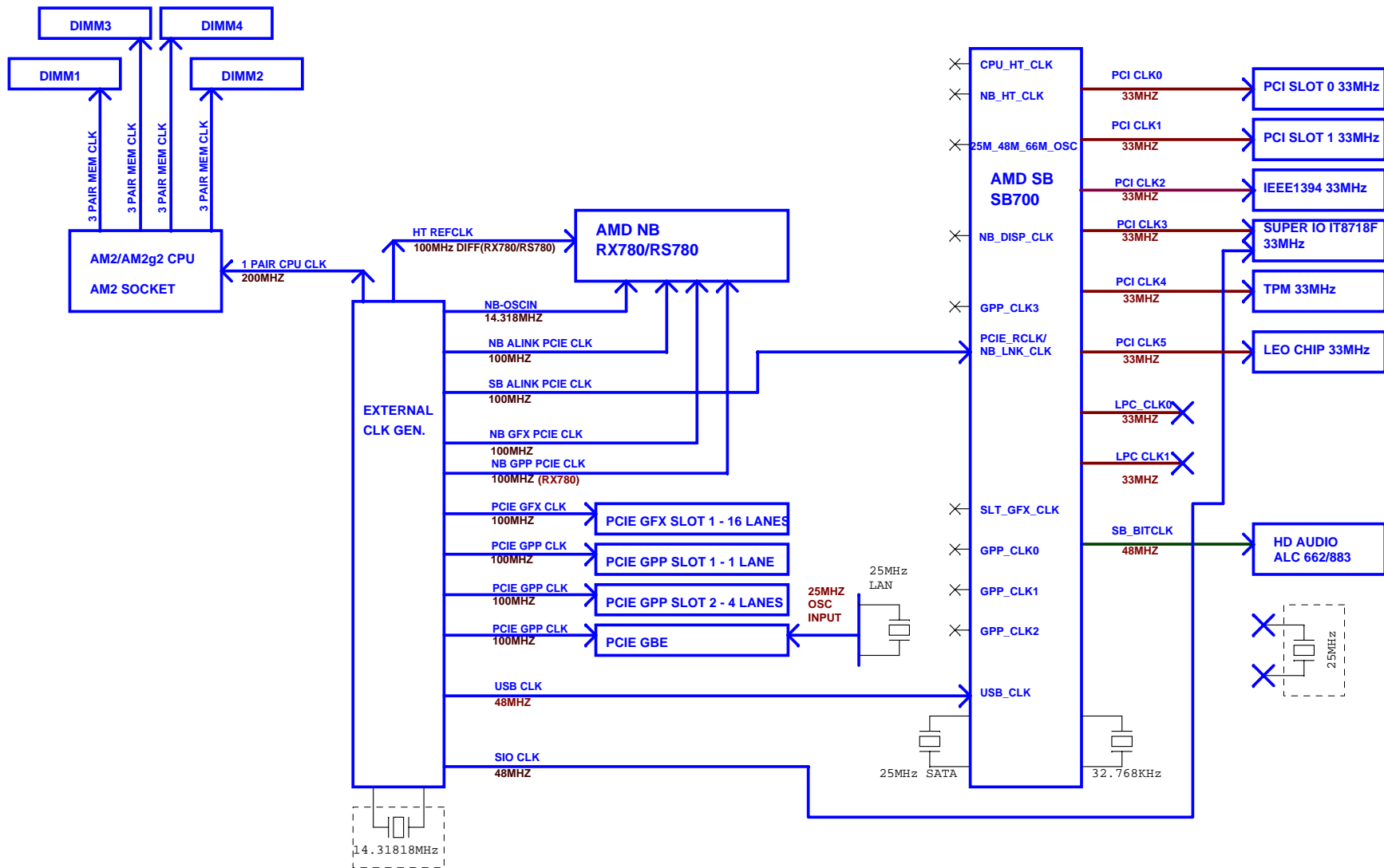
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI 2.3 Slot * 2

Intersil PWM:

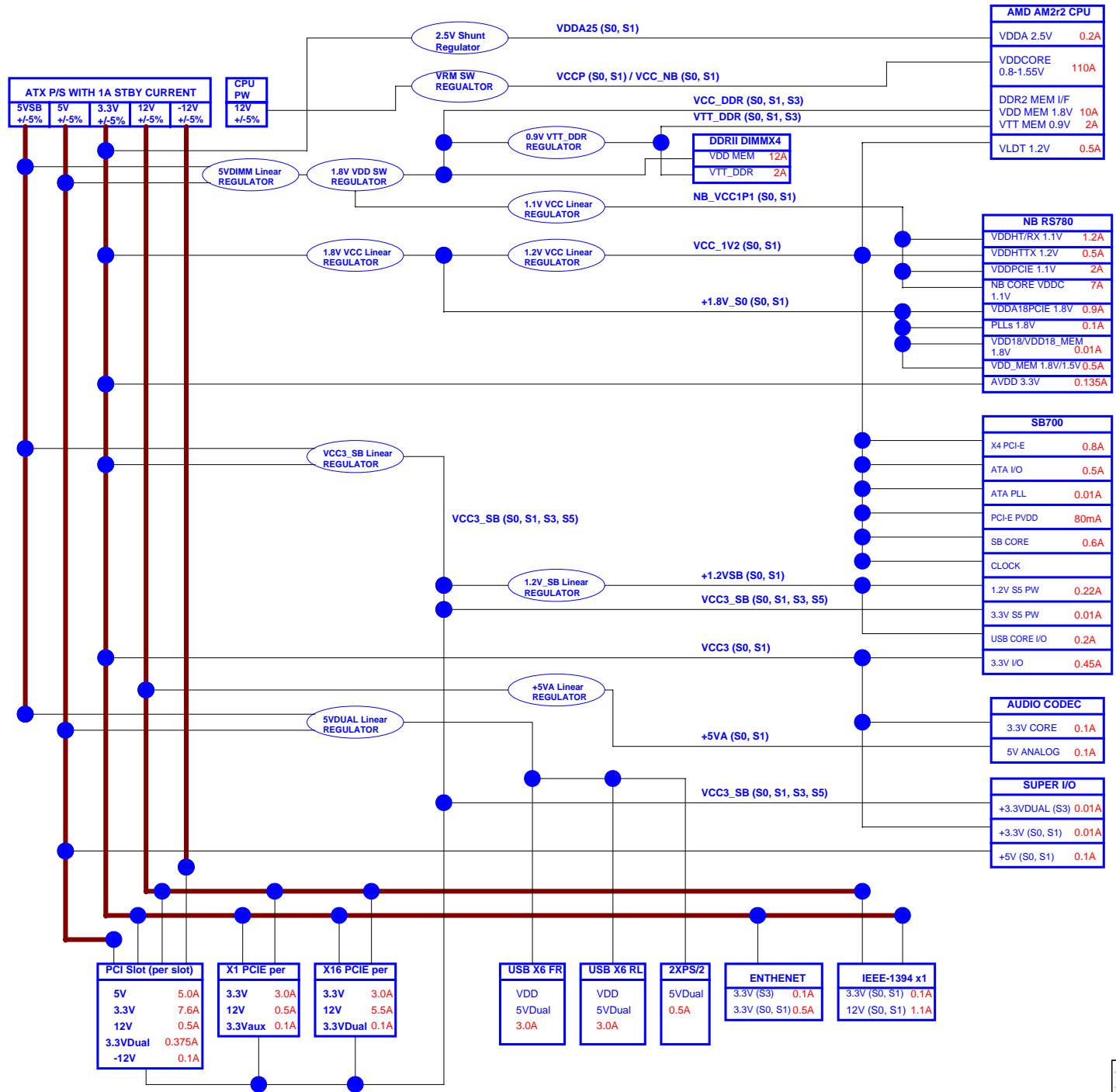
Controller - Intersil 6323 3 Phase

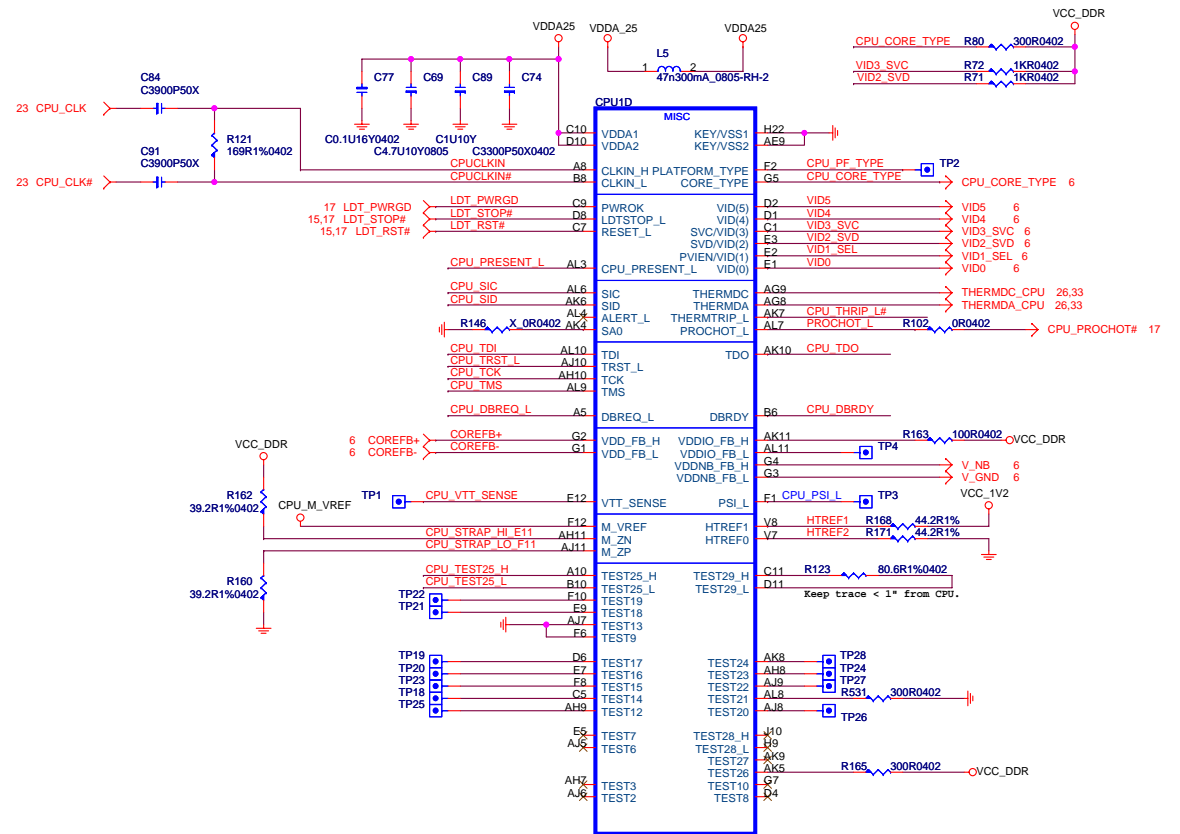
Project RS-780 BLOCK DIAGRAM



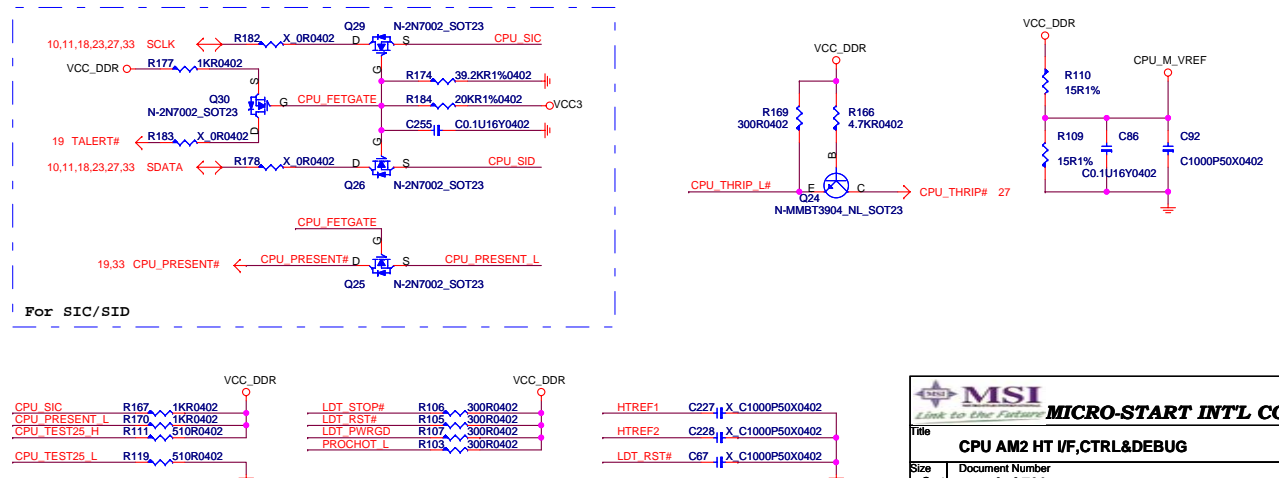


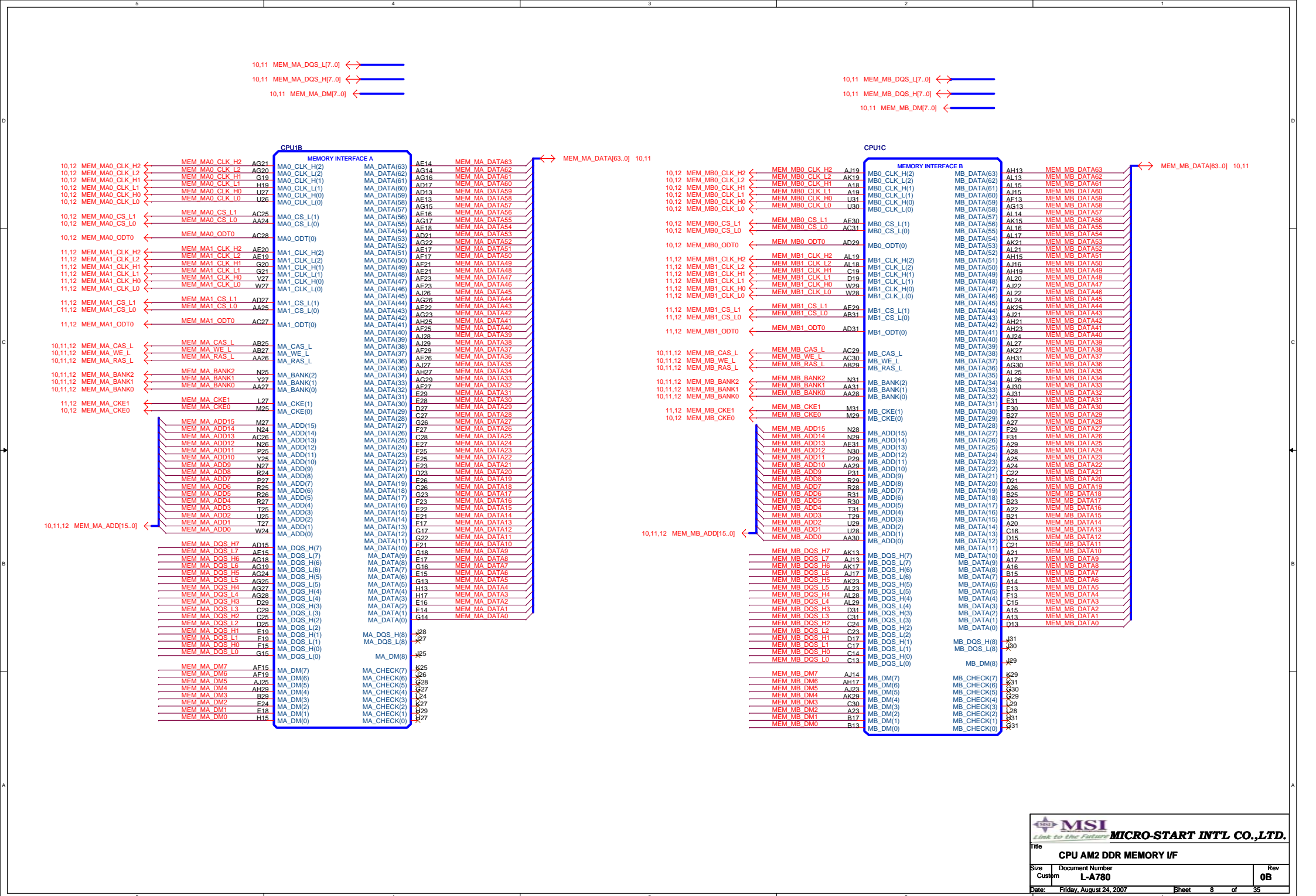
Power Deliver Chart

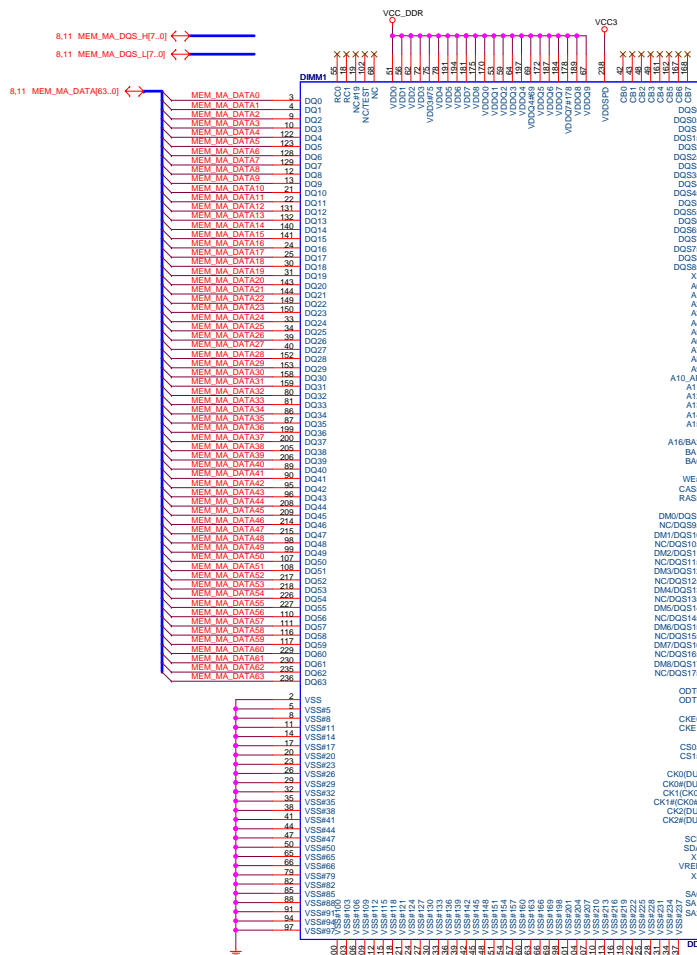




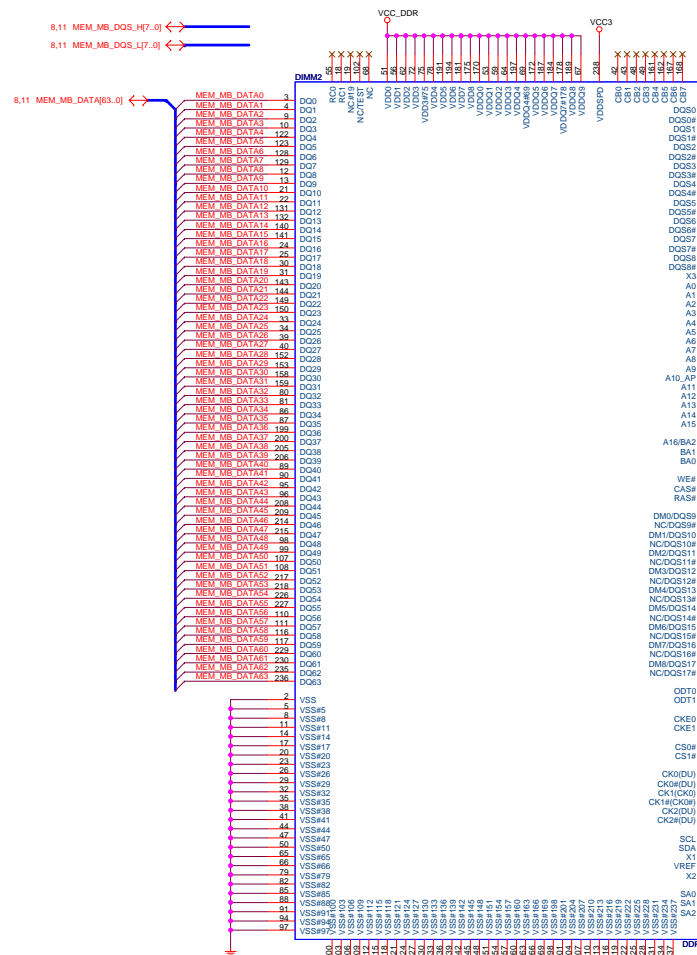
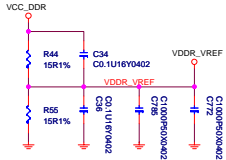
The schematic diagram illustrates the LDT_RST# signal path. The signal starts at SW1 (pin 1), passes through X_SW-TACT4PS (pin 3), X_100R0402 (R8), and Q1 (X_N-MMBT3904_NL_SOT23) to the LDT_RST# pin of J1 (X_H2X13[25]_black). The signal is also connected to VCC3 and VCC_DDR through resistors R22 (X_1KR0402) and R21 (X_4.7KR0402) respectively. The LDT_RST# signal is also connected to the LDT_RST_L pin of J1.



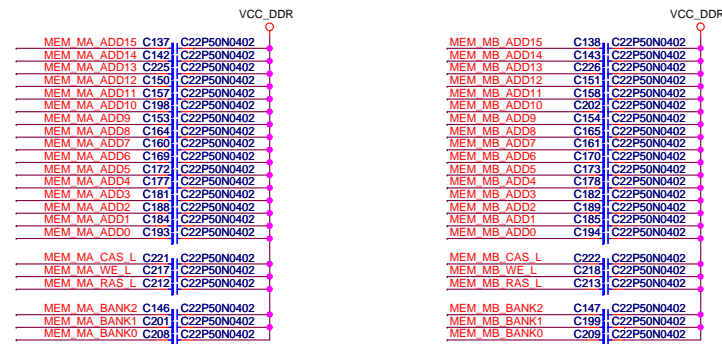
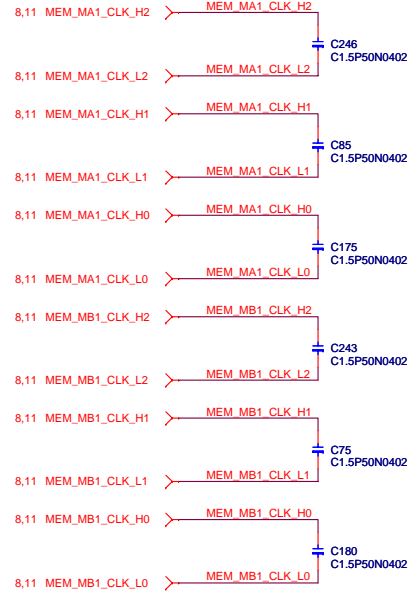
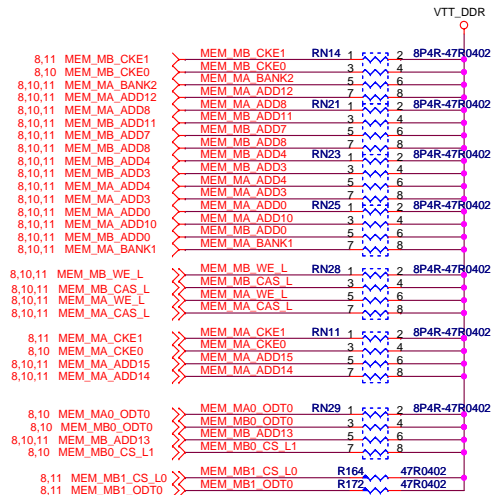
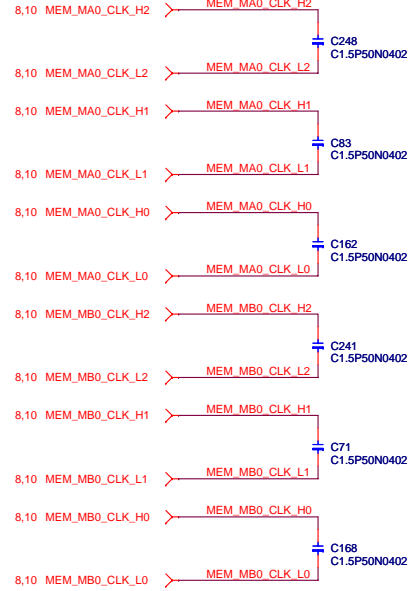
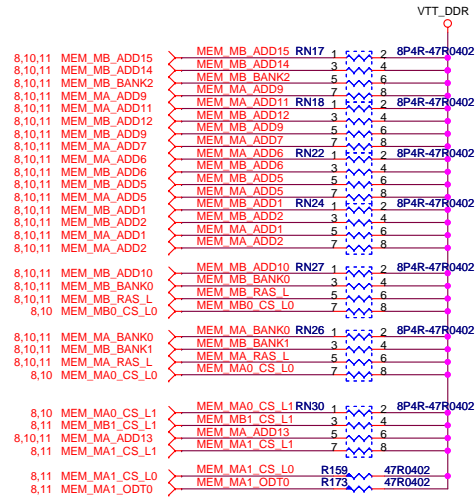




DIMM 1
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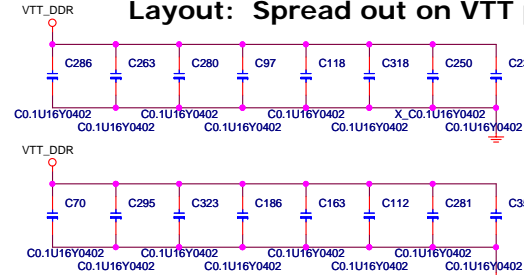


DIMM 2
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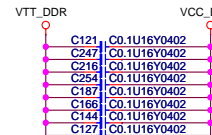
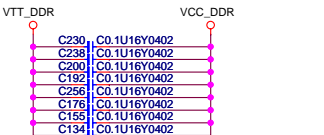
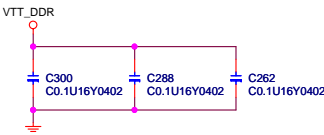
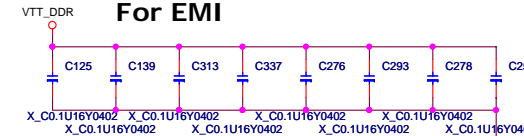


Decoupling Between Processor and DIMMs

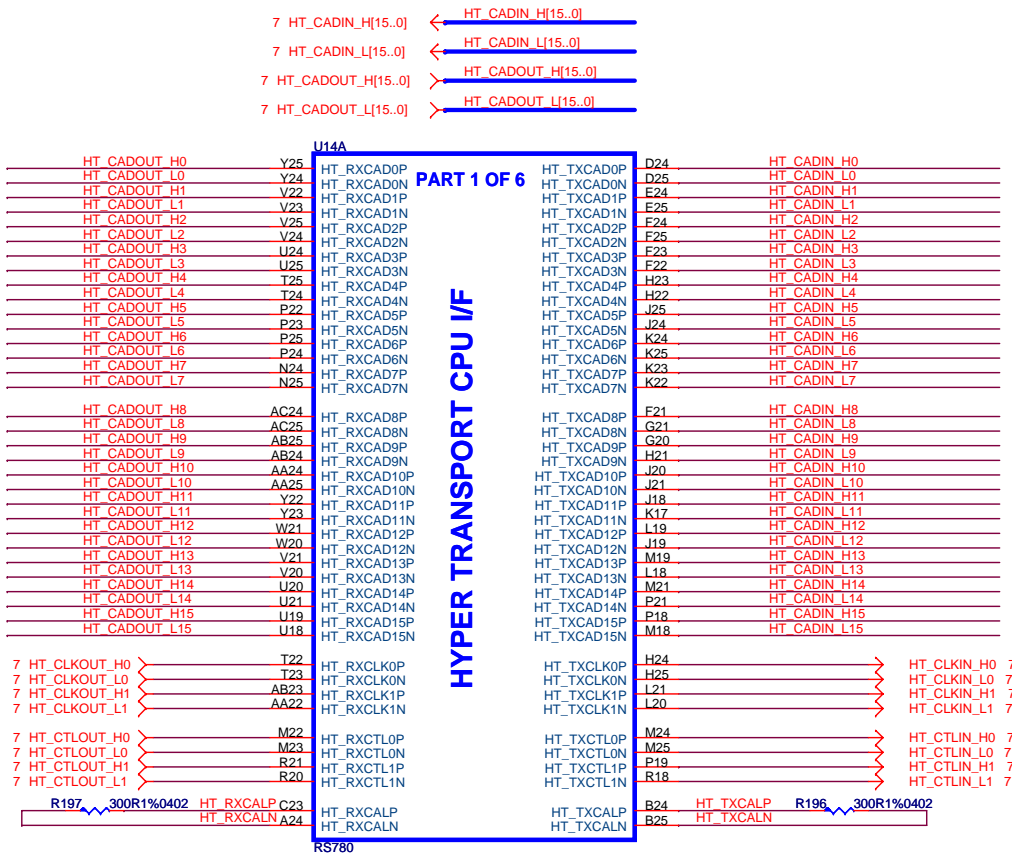
Layout: Spread out on VTT pour



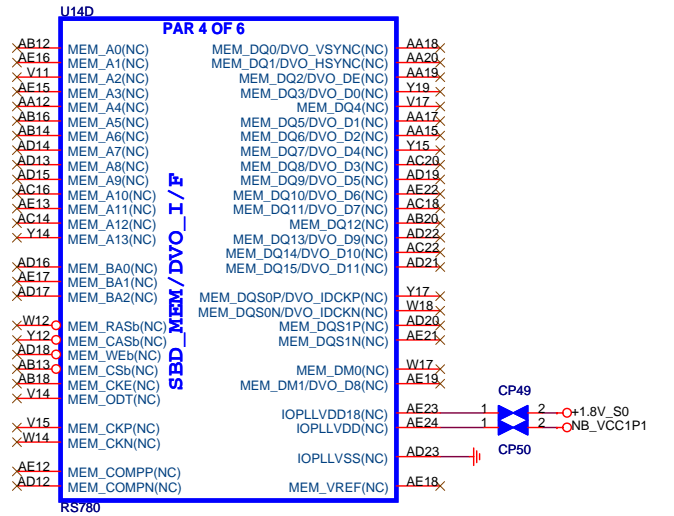
For EMI



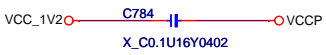
RS780-HT LINK I/F



HYPER TRANSPORT CPU I/F



Decoupling Cap for HT.



MSI

Link to the Future

MICRO-START INTL CO.,LTD.

Title

RS780-HT LINK I/F

Size B

Document Number

L-A780

Rev

0B

Date: Friday, August 24, 2007

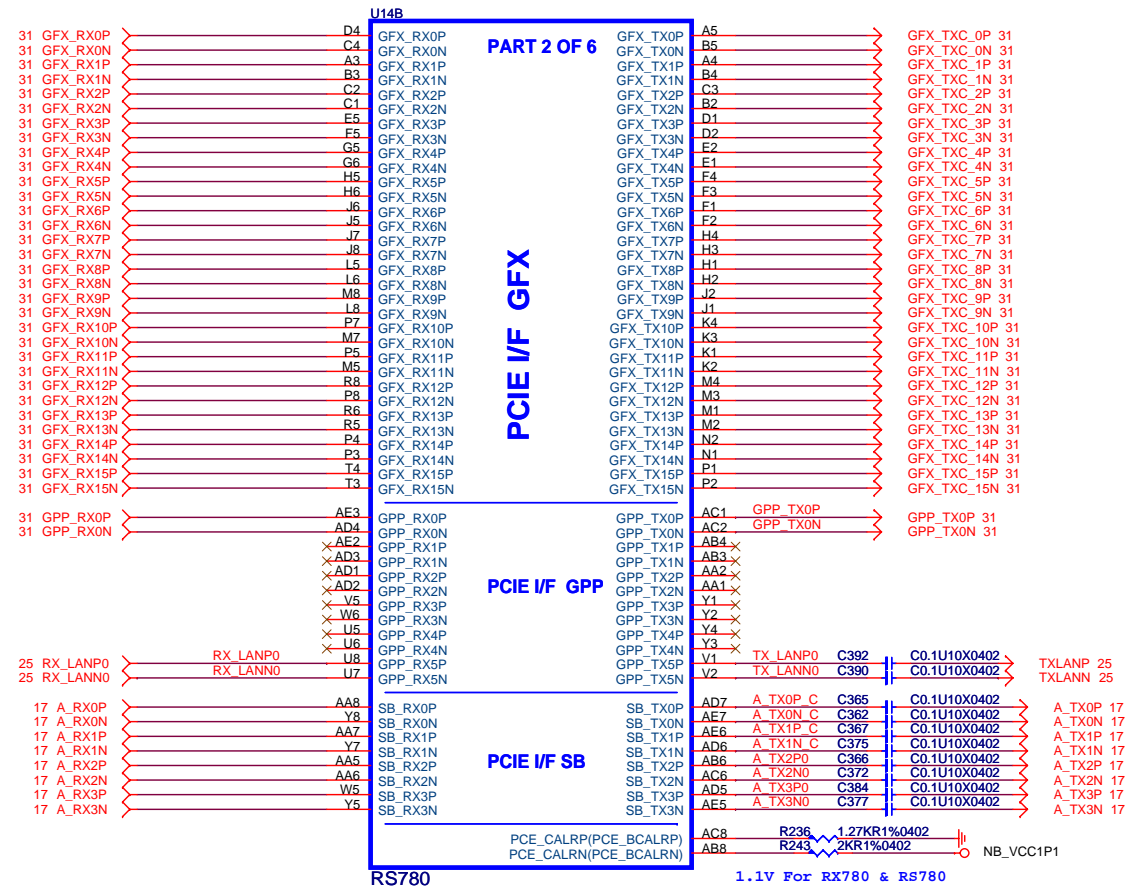
Sheet

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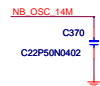
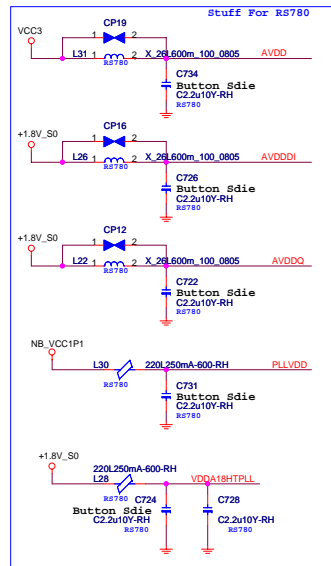
of

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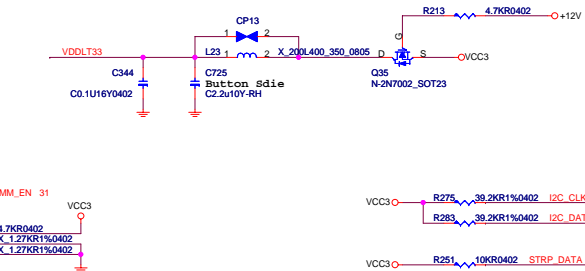
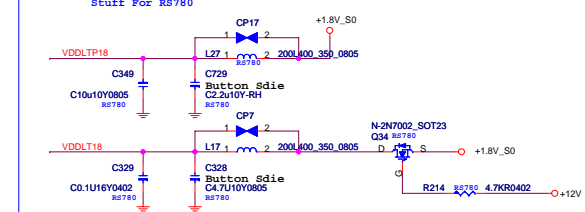
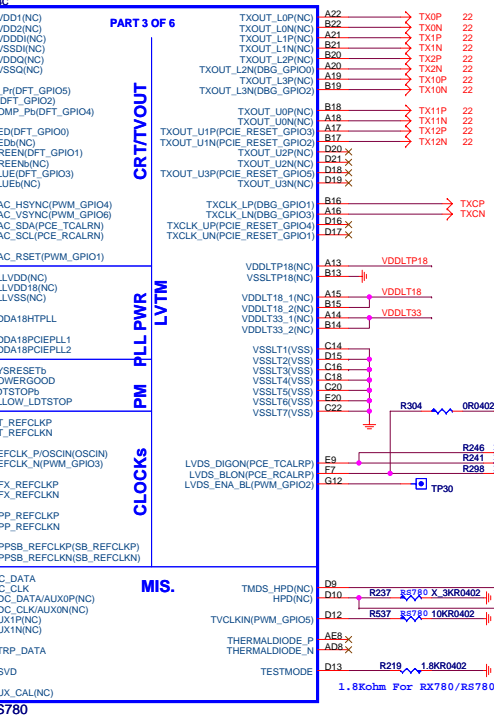
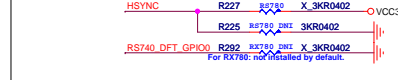
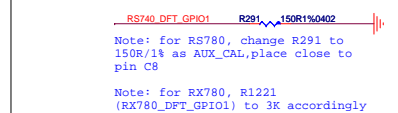
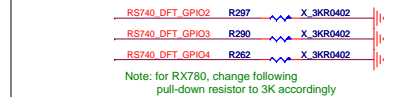
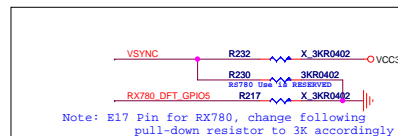
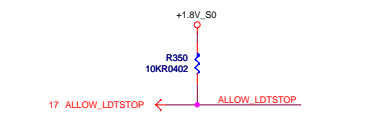
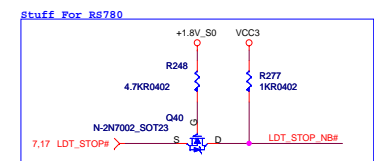
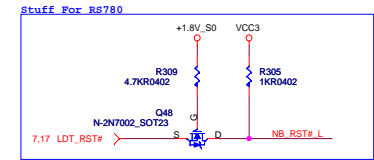
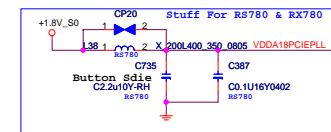
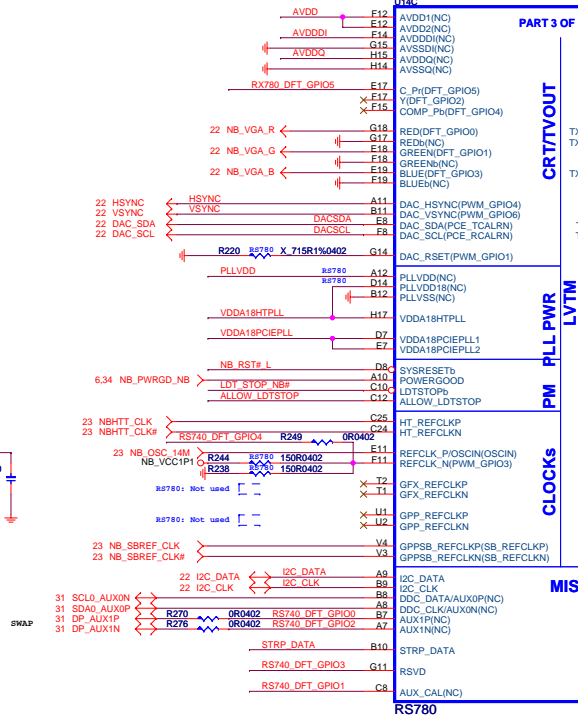
RS780-PCIE I/F



RS780-SYSTEM I/F



SWAP



RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLOK	LVDS_BLOK
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO

1 : Disable (RS740); Enable (RX780/RS780)

0 : Enable (RS740); Disable (RX780/RS780)

RS740: pin DFT_GPIO5

RX780: pin DFT_GPIO5

RS780: pin VSYNC

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

111: register defined (register default to Config E) default

110: 4-0-0-0-0 Config A

101: 4-4-0-0-0 Config B

100: 4-2-2-0-0 Config C

011: 4-2-1-1-0 Config D

010: 4-1-1-1-1 Config E

others: register defined (default to Config E)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740: pin DFT_GPIO1

RX780: pin DFT_GPIO1

RS780: pin SUS_STAT#

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory

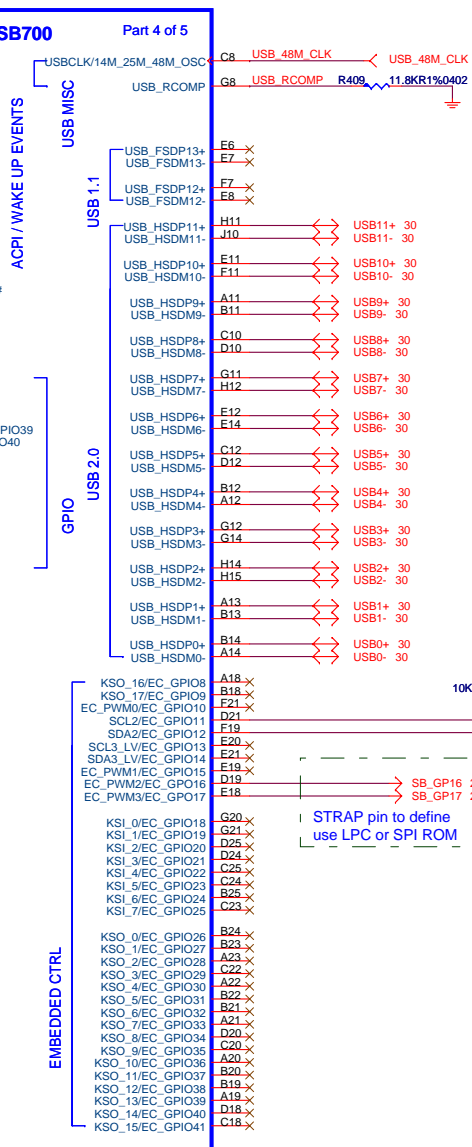
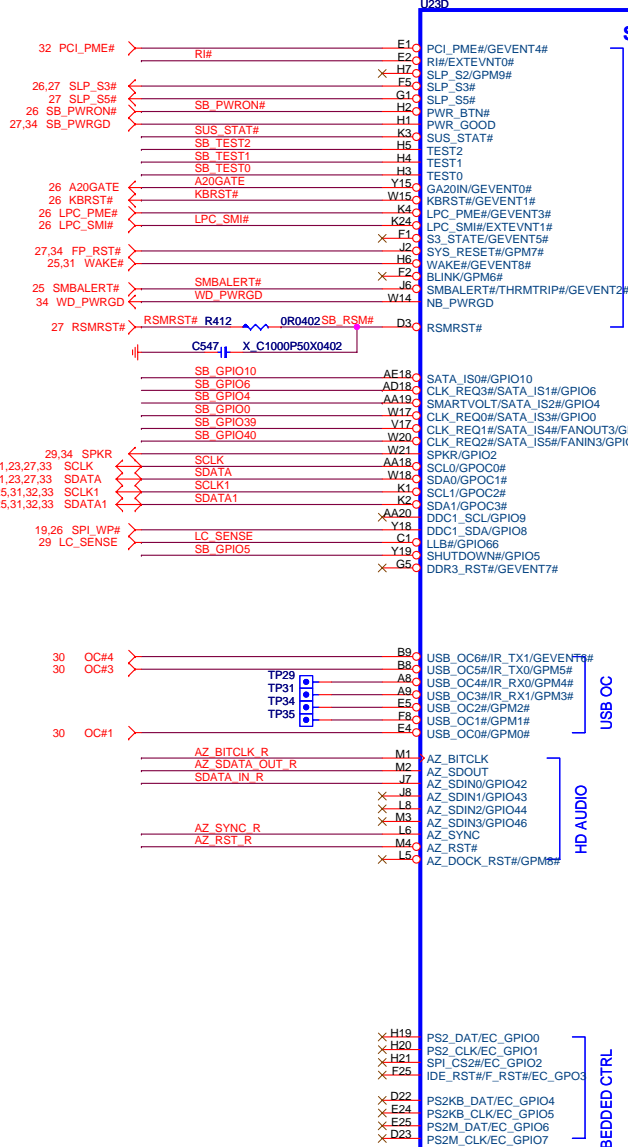
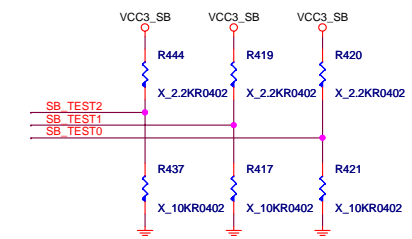
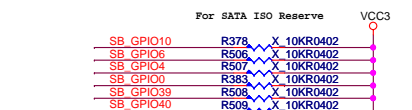
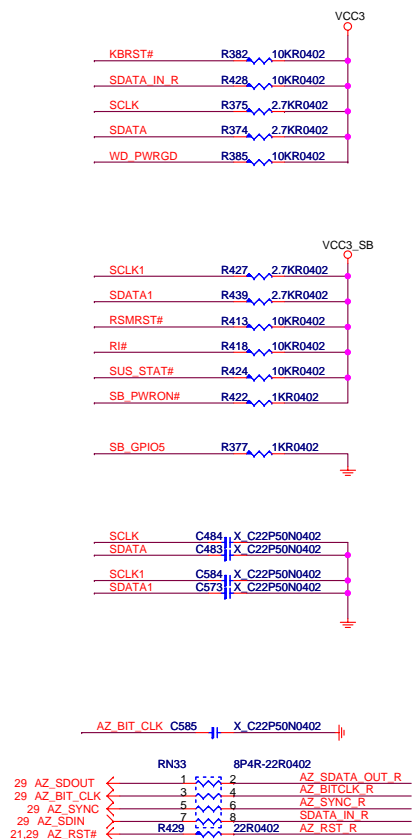
1: Disable (RS740/RS780)

0: Enable (RS740/RS780)

RS740: pin DFT_GPIO0

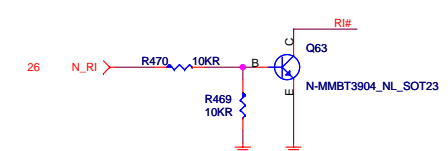
RS780: pin HSYNC

RX780: Not Applicable

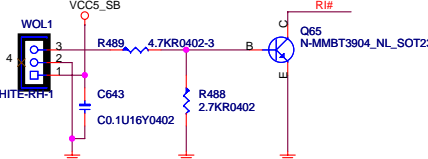


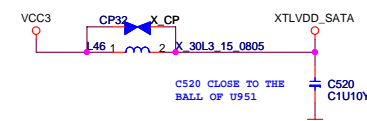
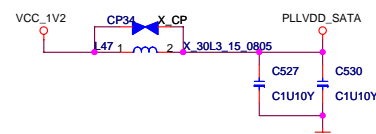
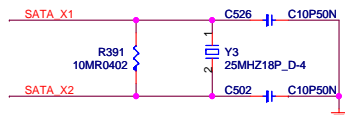
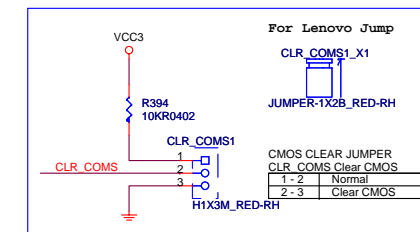
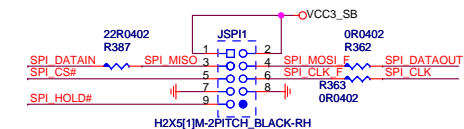
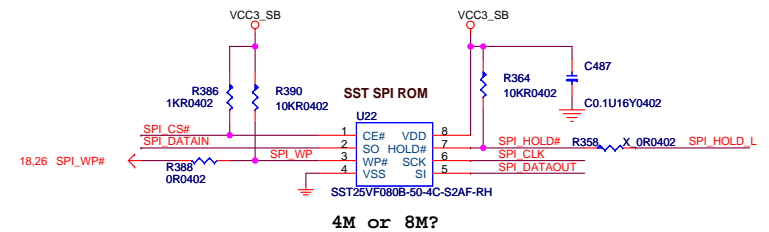
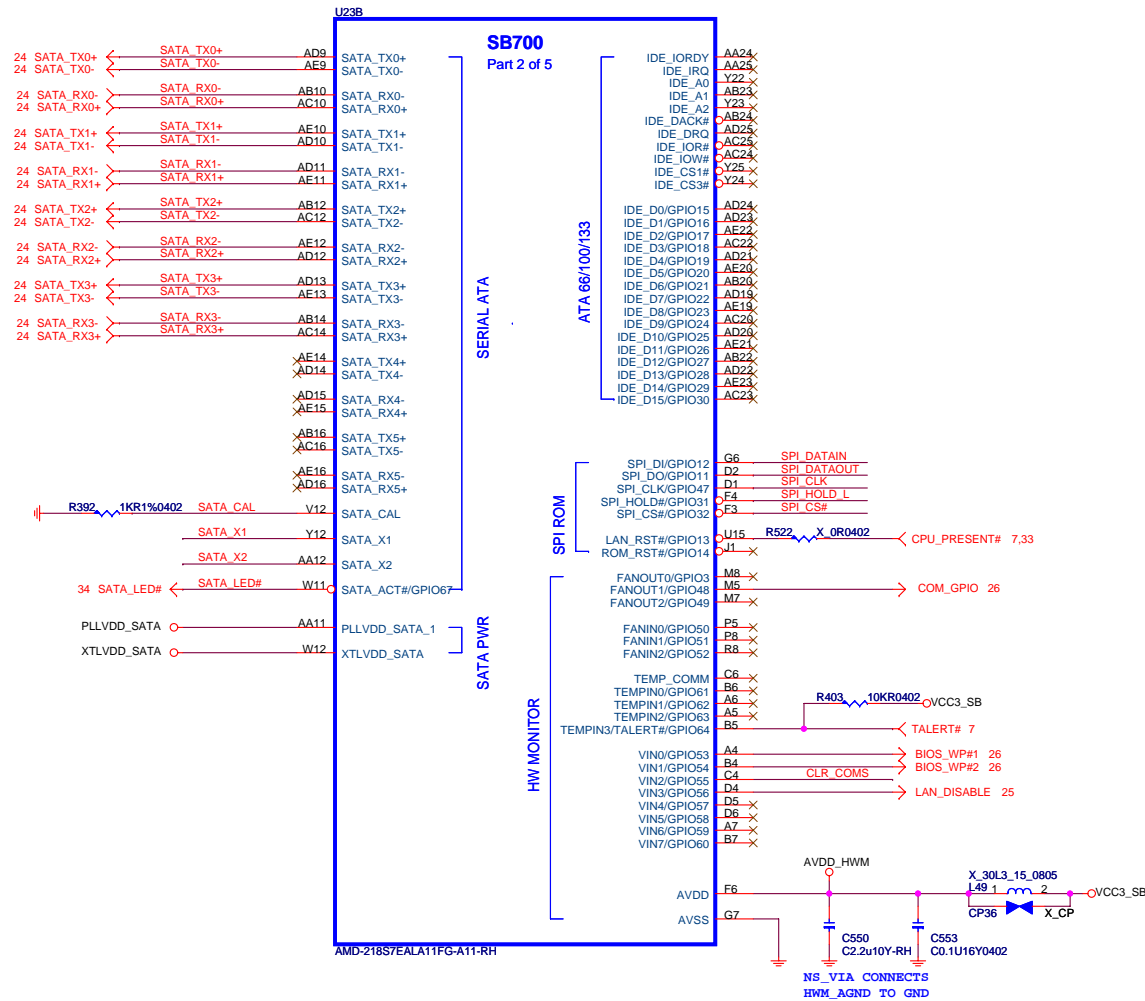
USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	STACK4 USB4
USB4	STACK4 USB3
USB3	STACK4 USB2
USB2	STACK4 USB1
USB1	LAN USB BOTTOM
USB0	LAN USB TOP

Wake On Modem Header



Wake on LAN

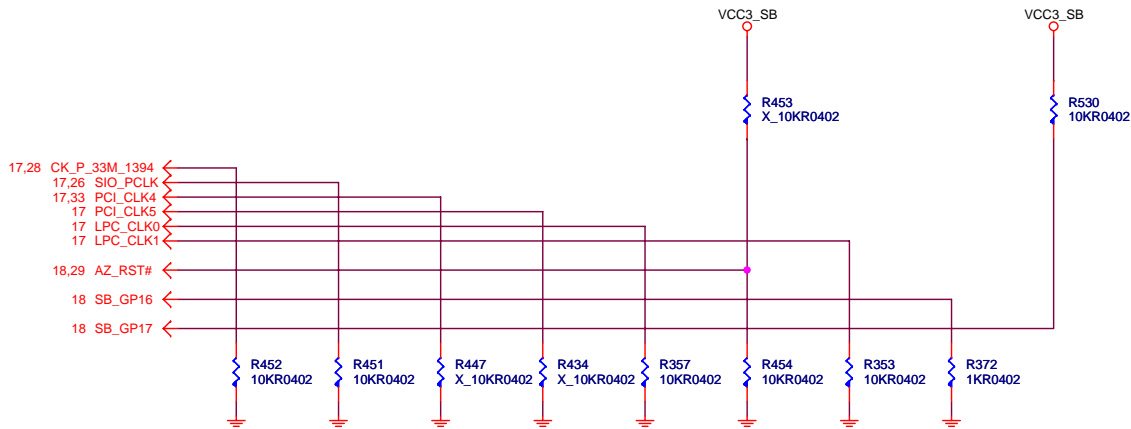







REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



	PCI_CLK2 CK_P_33M_1394	PCI_CLK3 SIO_PCLK	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16	
	Watchdog timer on NB_PWGRD	Debug straps	TPM CLOCK	RESERVED	Booting from PCI Memory	Internal Clock Generator	INTERNAL RTC	EC ENABLED	ROM TYPE: NC, NC = Reserved NC, L = SPI ROM DEFAULT L, NC = LPC ROM L, L = FWH ROM Note: NC represents internal 10-k? 5% pull-up	
PULL HIGH	ENABLED (VCC3)	ENABLED (VCC3)			ENABLED (VCC3_SB)	ENABLED (VCC3_SB)		ENABLED		
PULL LOW	DISABLED DEFAULT	DISABLED DEFAULT			DISABLED DEFAULT	DISABLED DEFAULT	NC IS EXT. RTC DEFAULT	DISABLED DEFAULT		



MICRO-START INTL CO.,LTD.

Title

SB700 STRAPS

Size B

Document Number

Rev

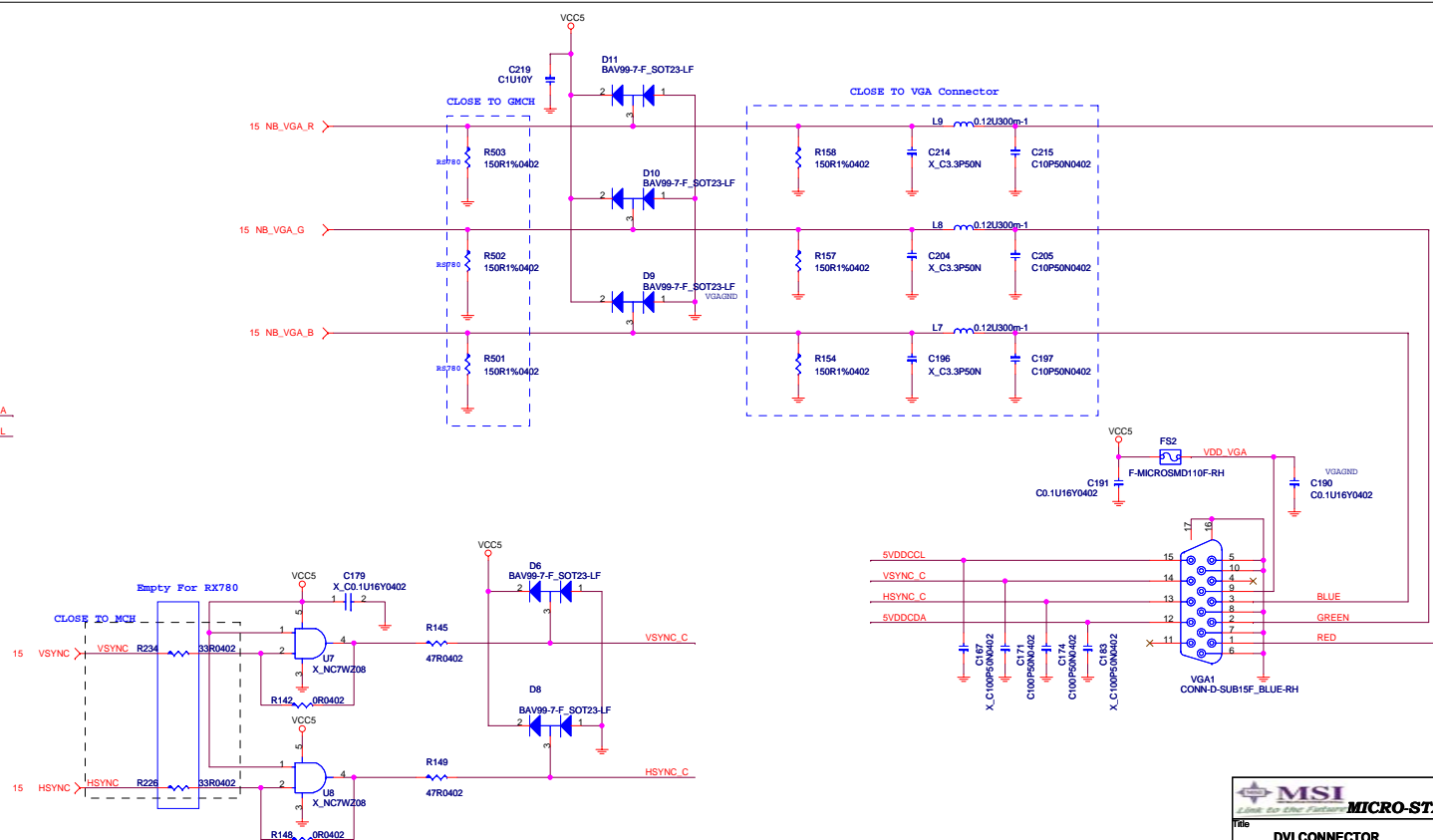
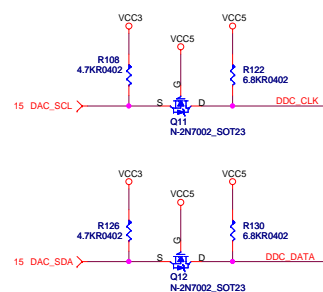
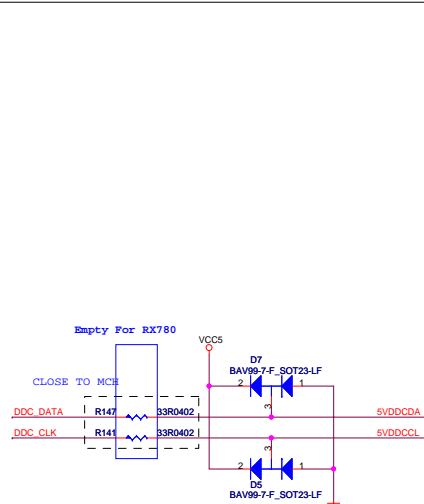
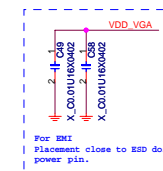
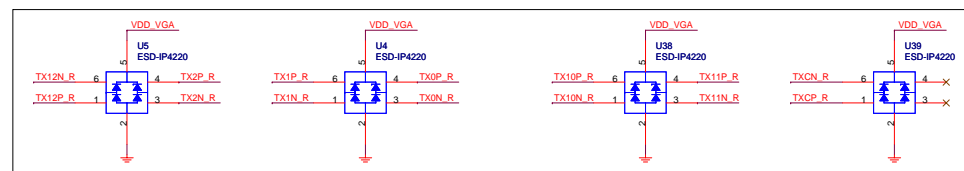
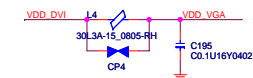
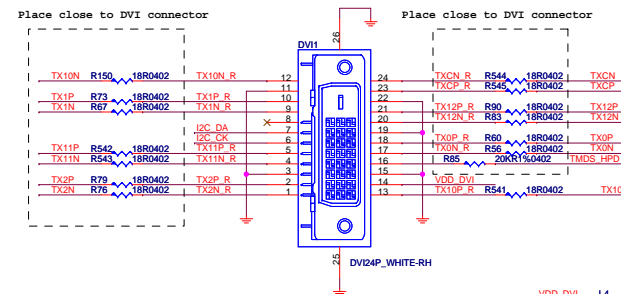
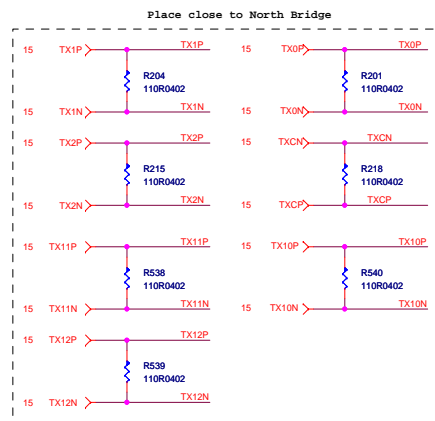
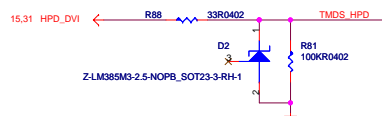
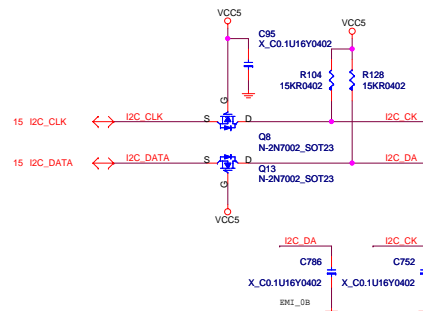
L-A780

0B

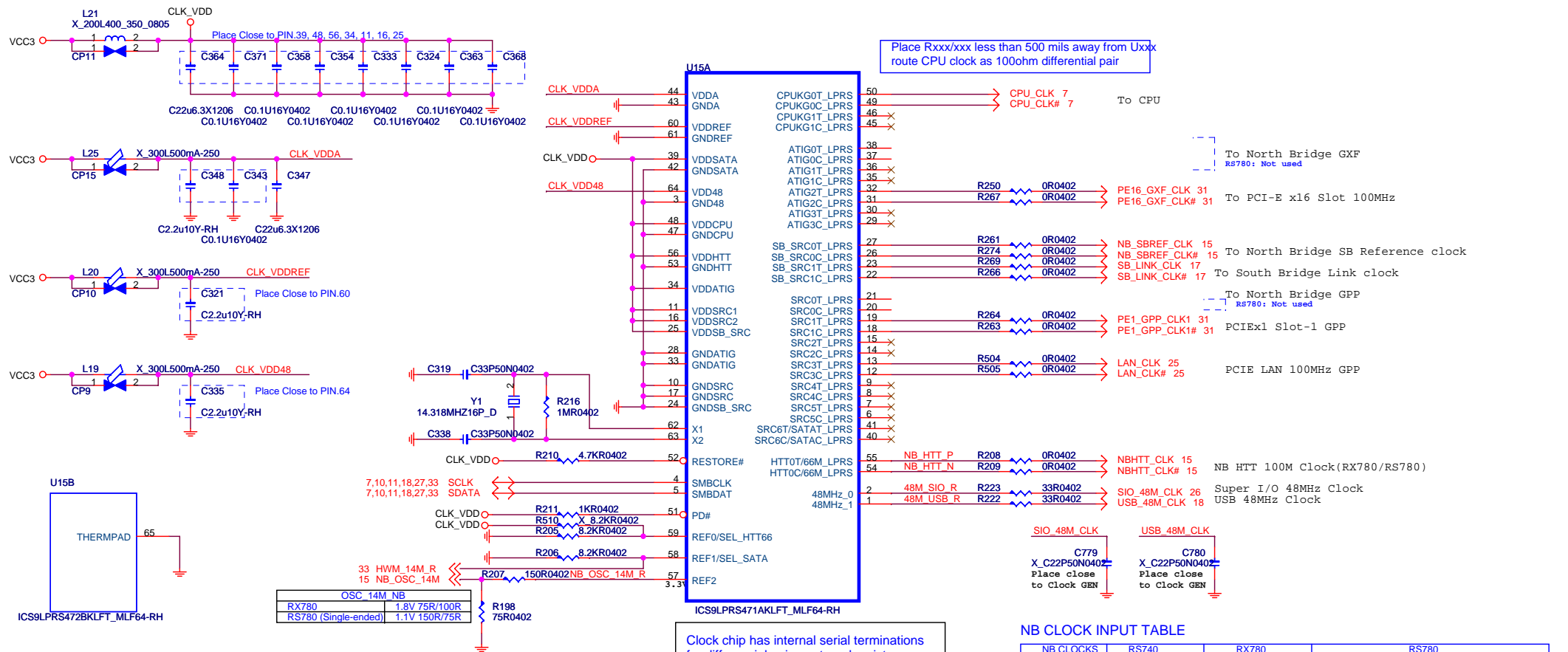
Date: Friday, August 24, 2007

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DVI CONNECTOR



Clock Gen ICS9LPR472




REF0/SEL_HTT66	HTT CLOCK	REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL	0	100.00 DIFFERENTIAL SPREADING SRC CLCOK
1	66.66 SINGLE END	1	100.00 NON-SPREADING DIFFERENTIAL SATA CLCOK

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPSPS_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

**MICRO-START INT'L CO.,LTD.**

Clock Gen ICS9LPR472

Size B

Document Number
L-A780

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0B

Date: Tuesday, August 28, 2007

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Figure 10 shows the pin connections for SATA1, SATA2, SATA3, and SATA4. Each diagram includes a 15-pin SATA connector with its internal wiring to a SATA7PM chip. The connections are as follows:

- SATA1:**
 - SATA_TX0+ to C589, C588 to C590, C591 to C592, C593 to C594, C595 to C596, C597 to C598, C599 to C600, C601 to C602, C603 to C604, C605 to C606, C607 to C608, C609 to C610, C611 to C612, C613 to C614, C615 to C616, C617 to C618, C619 to C620, C621 to C622, C623 to C624, C625 to C626, C627 to C628, C629 to C630, C631 to C632, C633 to C634, C635 to C636, C637 to C638, C639 to C640, C641 to C642, C643 to C644, C645 to C646, C647 to C648, C649 to C650, C651 to C652, C653 to C654, C655 to C656, C657 to C658, C659 to C660, C661 to C662, C663 to C664, C665 to C666, C667 to C668, C669 to C670, C671 to C672, C673 to C674, C675 to C676, C677 to C678, C679 to C680, C681 to C682, C683 to C684, C685 to C686, C687 to C688, C689 to C690, C691 to C692, C693 to C694, C695 to C696, C697 to C698, C699 to C700, C701 to C702, C703 to C704, C705 to C706, C707 to C708, C709 to C710, C711 to C712, C713 to C714, C715 to C716, C717 to C718, C719 to C720, C721 to C722, C723 to C724, C725 to C726, C727 to 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[illegible][illegible]

The schematic diagram illustrates the SYSFAN control circuit. It features a +12V power supply connected to a network of resistors (R233, R235, R245, R199, R200) and capacitors (C314, C359, EC33). A MOSFET driver stage is composed of a P-MOSFET (Q36) and an N-MOSFET (Q37). The driver is controlled by the SYSFAN_PWM signal. The fan motor (BH1X48_Brown-RH) is connected to the MOSFETs. The circuit also includes a current sense resistor (R200) and a sense amplifier (C359). The fan speed is monitored by a tachometer signal (FAN2_DRV) and a sense signal (FAN2_SEN).

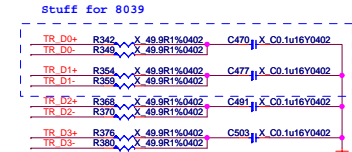
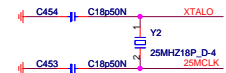
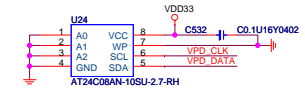
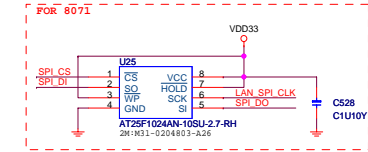
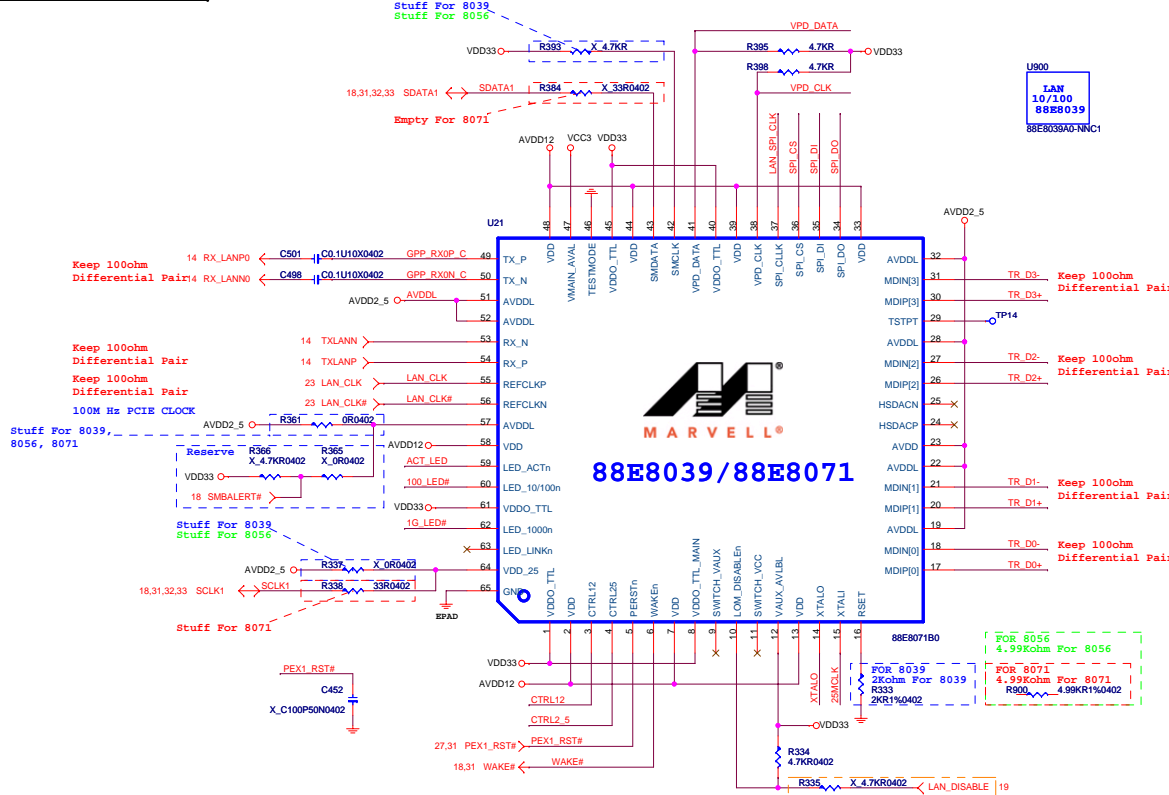
LAN-Marvell 88E8039/8056/8071/8075

FOR 8039
B06-080390C-M44
Ver:1.0

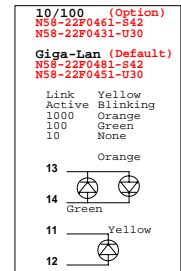
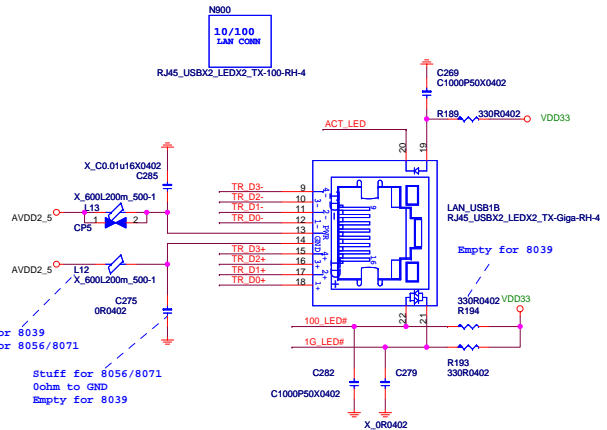
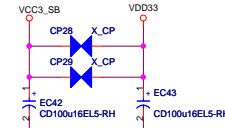
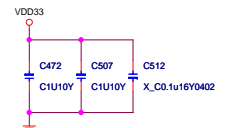
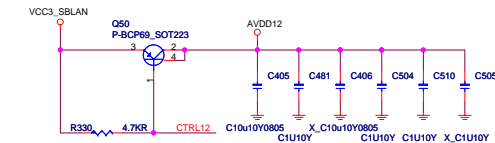
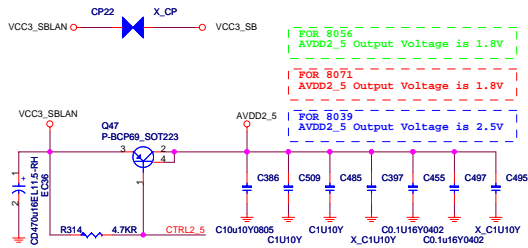
FOR 8056
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Ver:1.0

FOR 8071
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Ver:1.0

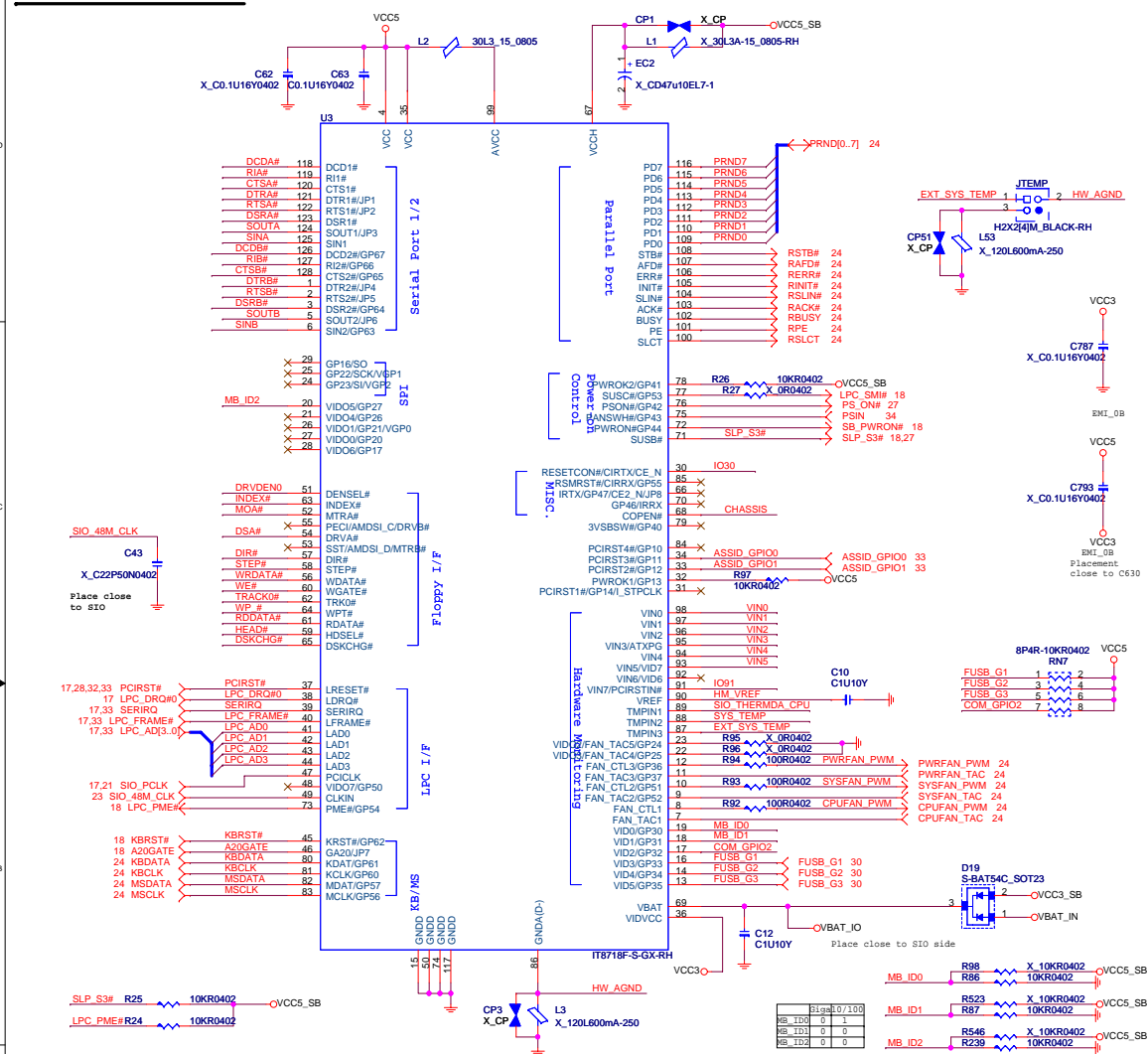
FOR 8070(Default)
B06-080700C-M44
Ver:1.0



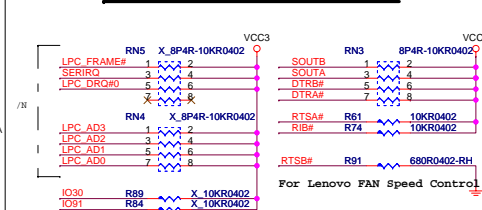
All Stuff for 8056
All Empty for 8071(Default)



LPC I/O IT8718F



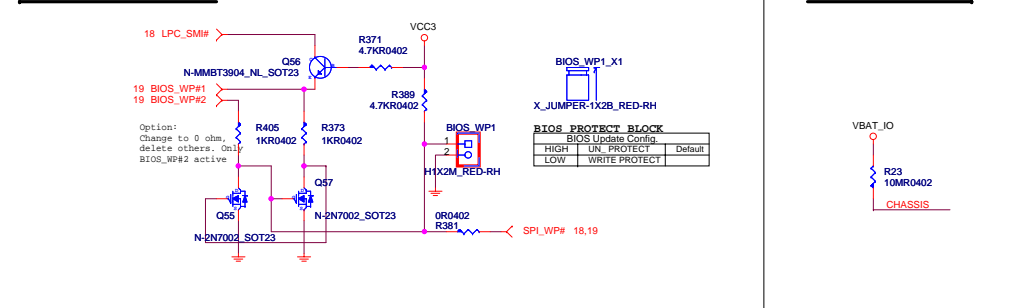
SUPER I/O STRAPPING RESISTOR



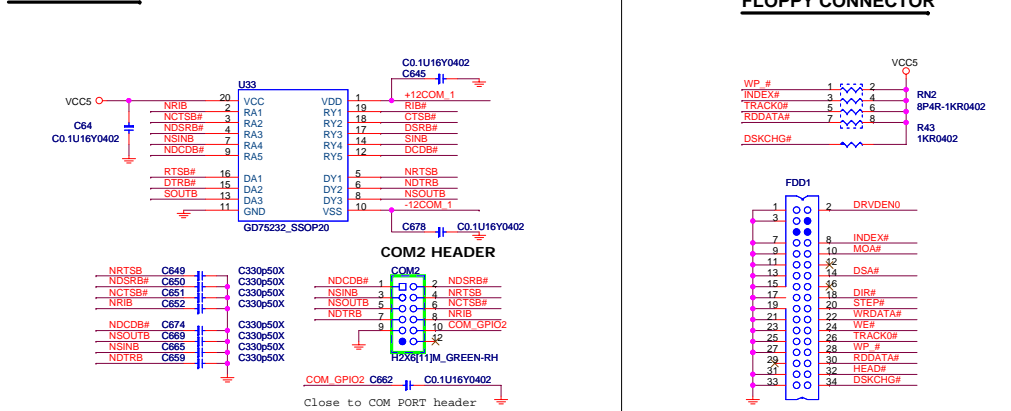
Power On Strapping Options

Symbol	value	Description
Flashseg1_EN	1	Disabled.
	0	Flash I/F Address Segment 1 (FFFF_0000h-FFFF_FFFFh, 000F_0000h-000F_FFFFh) is enabled
VIDO_SEL	1	Disable VIDOUT pins(except VIDO6 & VIDO7)
	0	Enable VIDOUT pins
CHIP_SEL	--	Chip selection in configuration.
BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
	0	The output buffers are push-pull.
FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
	0	The default value of EC Index 15h / 16h / 17h is 40h
VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
	0	The threshold voltage of VID is 0.8 / 0.4V

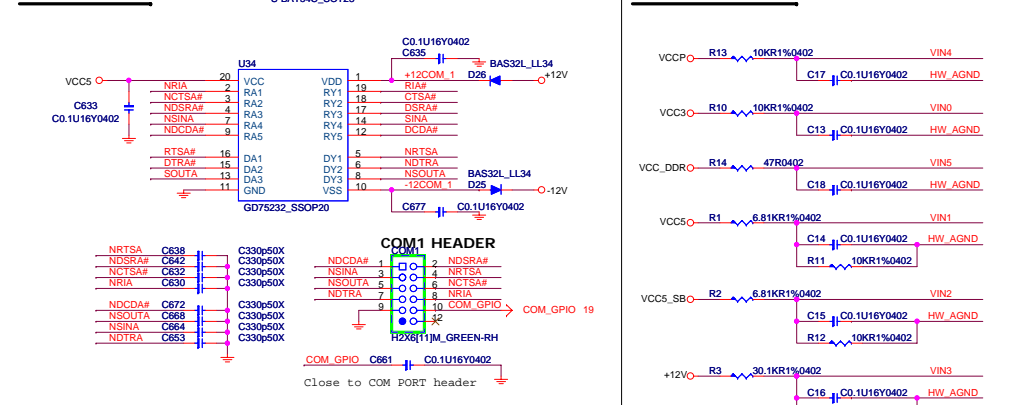
BIOS WRITE PROTECT



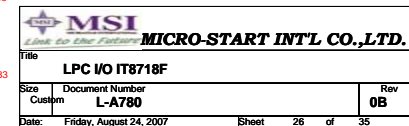
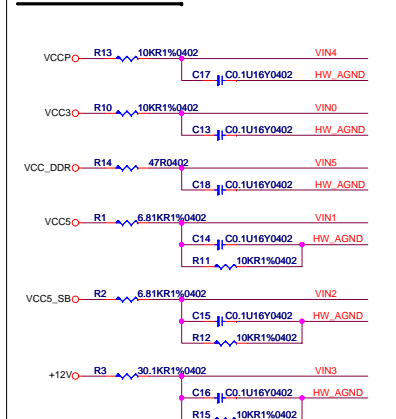
SERIAL PORT 2



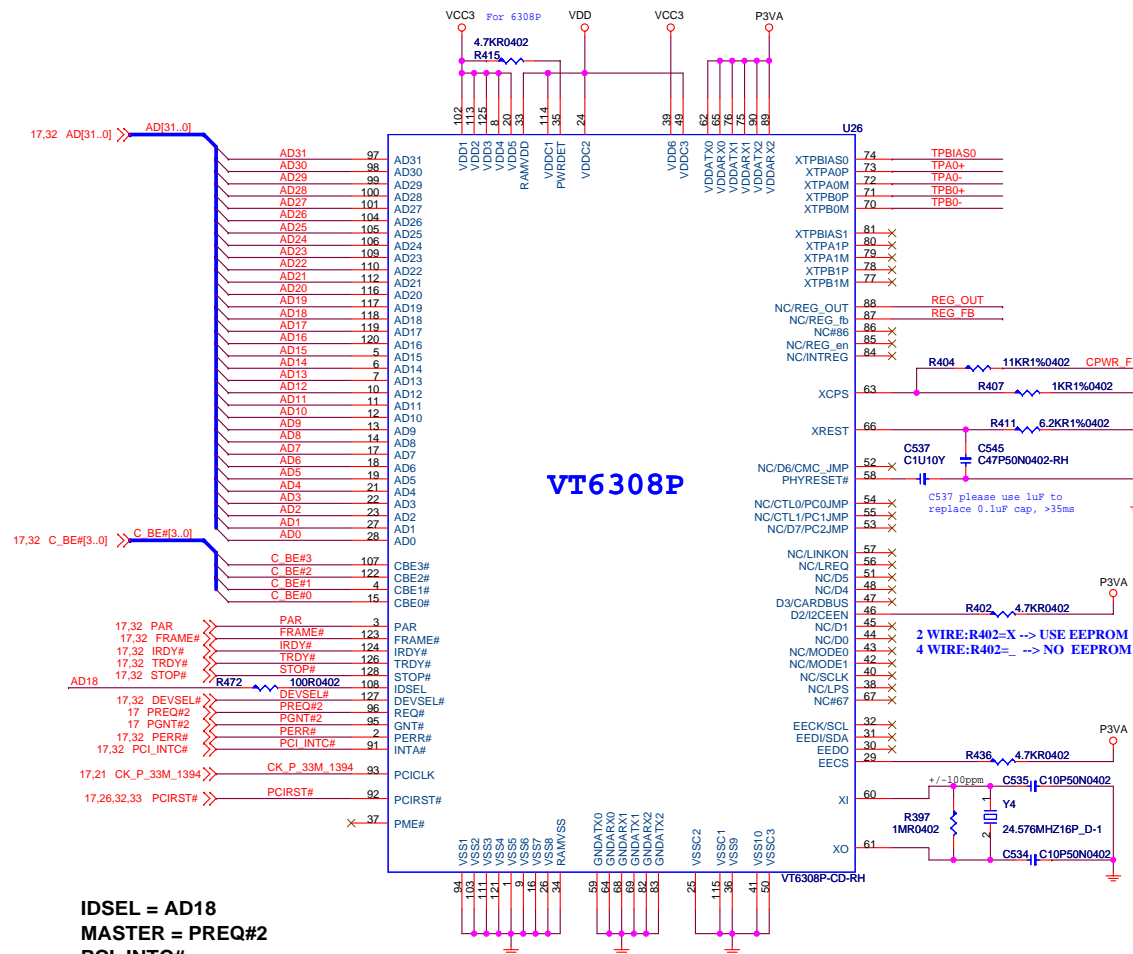
SERIAL PORT 1



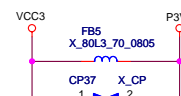
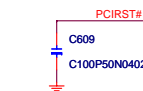
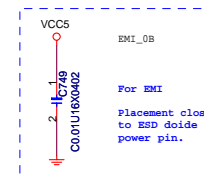
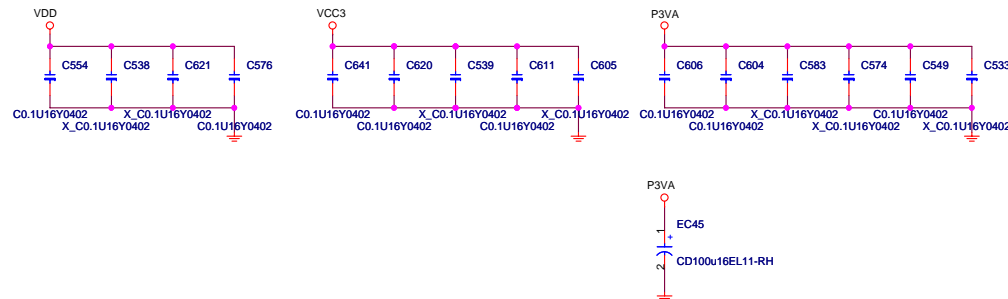
Thermal Resistor



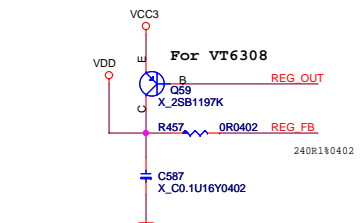
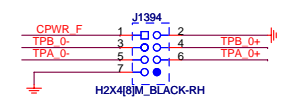
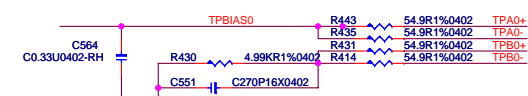
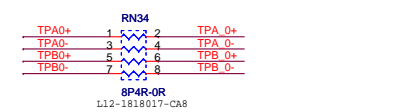
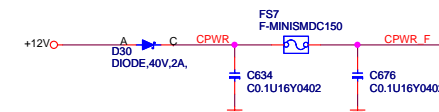
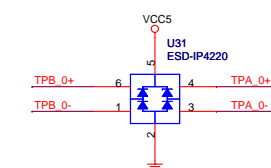
IEEE-1394 VT6308P



IDSEL = AD18
MASTER = PREQ#2
PCI_INT#
PCICLK#2

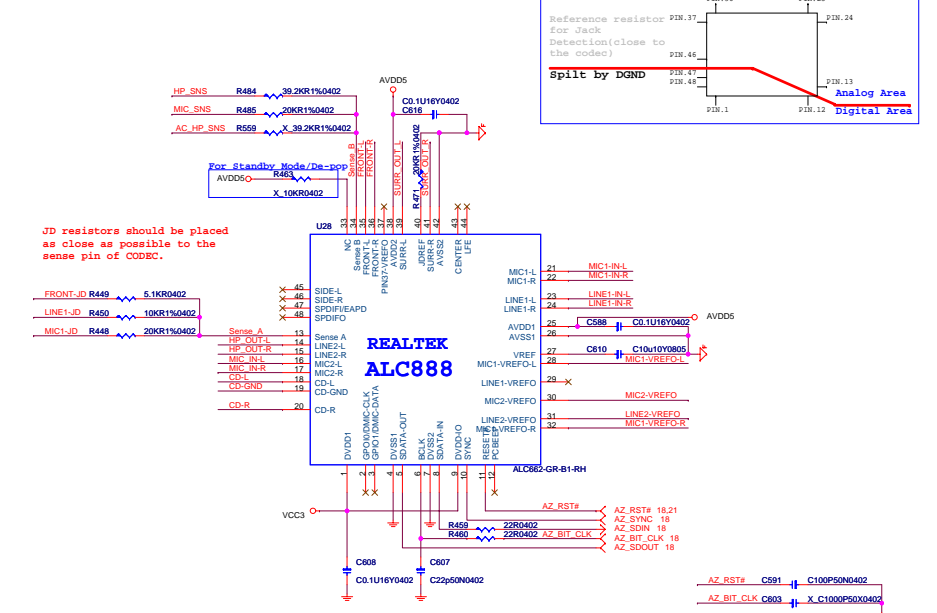


For IEEE-1394 ESD

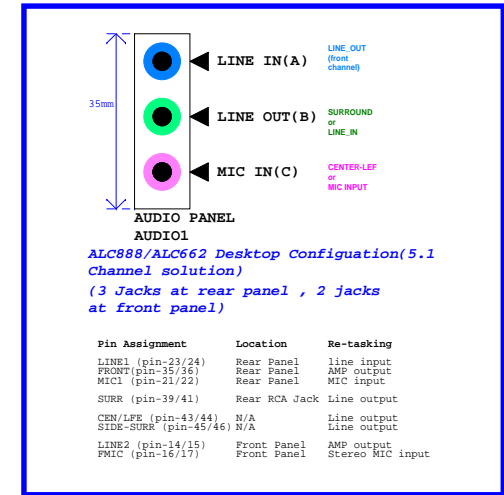
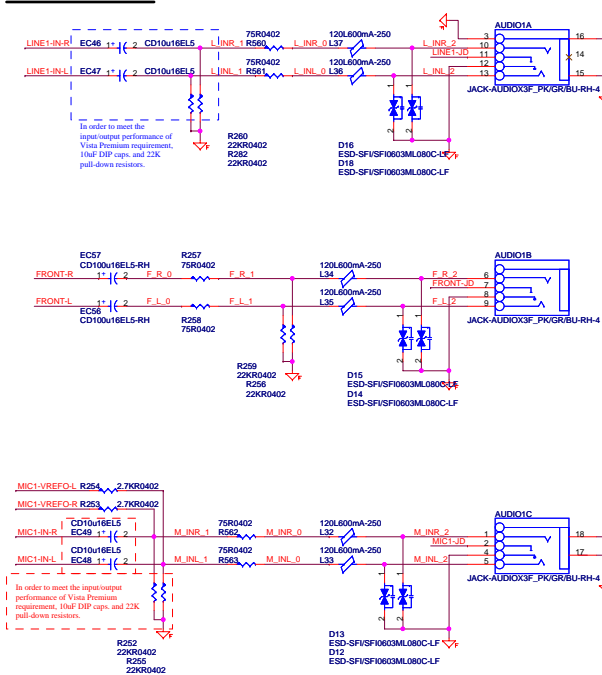


Audio Codec ALC662 (ALC888)

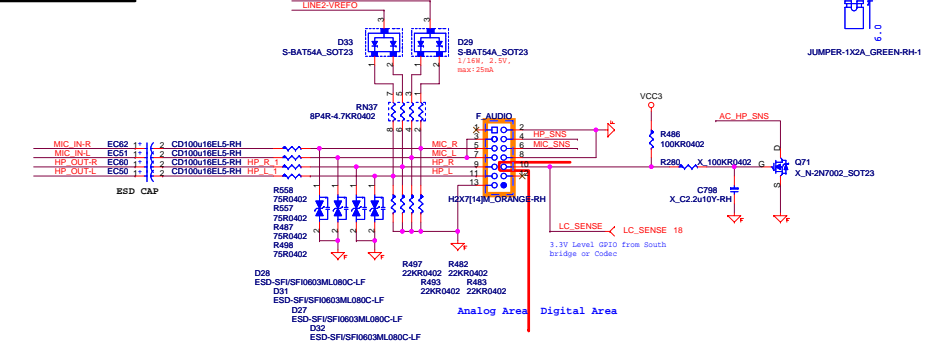
Default is ALC662



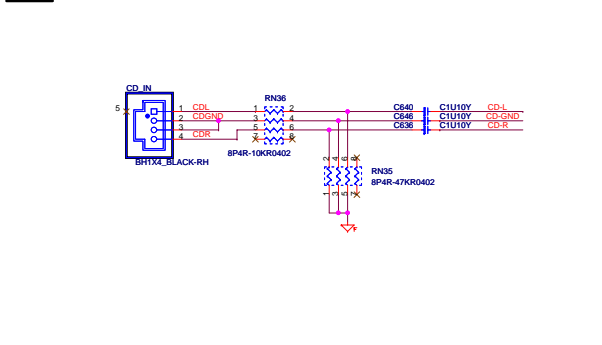
Rear Phone Jack



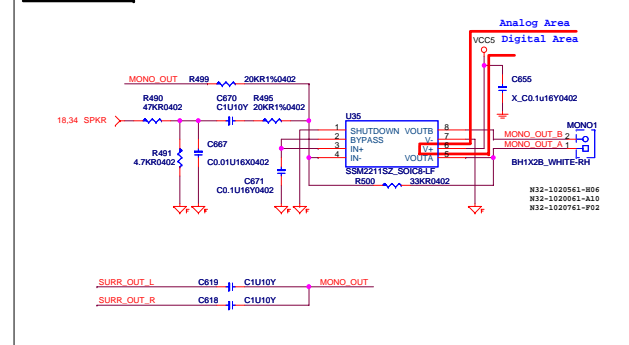
Front Audio Jack



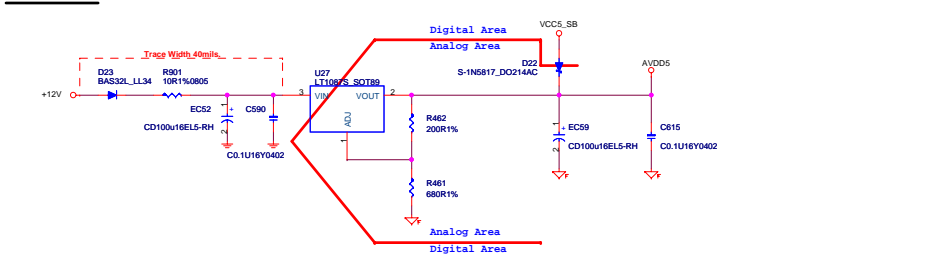
CD IN



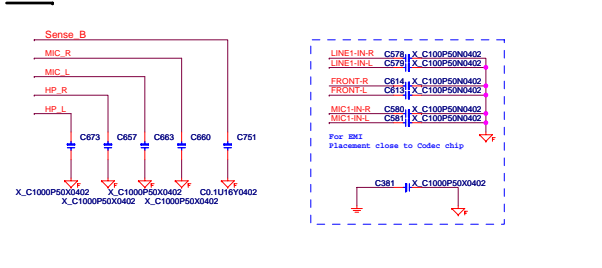
MONO Amplifier



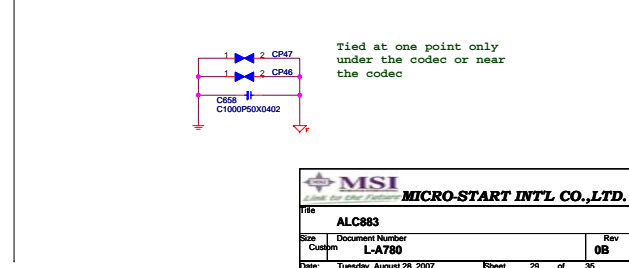
Audio Power



EMT

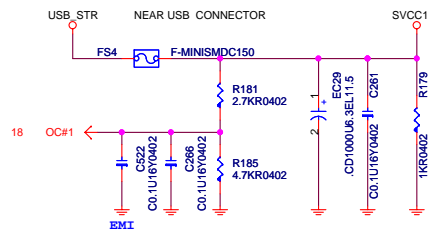


MONO Amplifier



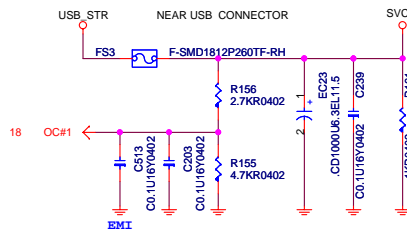
POWER CIRCUIT FOR USB PORT 0,1

Rear



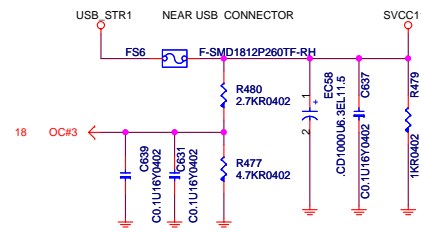
POWER CIRCUIT FOR USB PORT 2,3,4,5

Rear



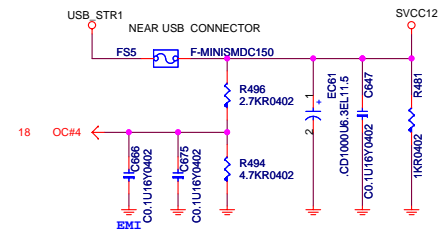
POWER CIRCUIT FOR USB PORT 6,7,8,9

Front

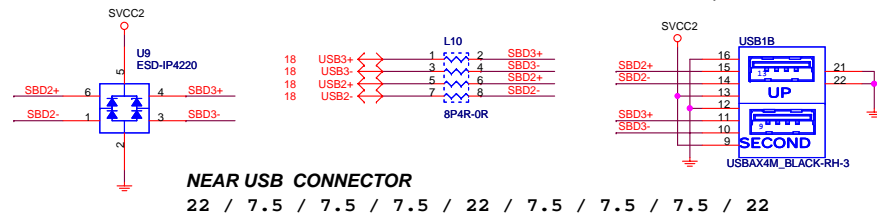


POWER CIRCUIT FOR USB PORT 10,11

Front

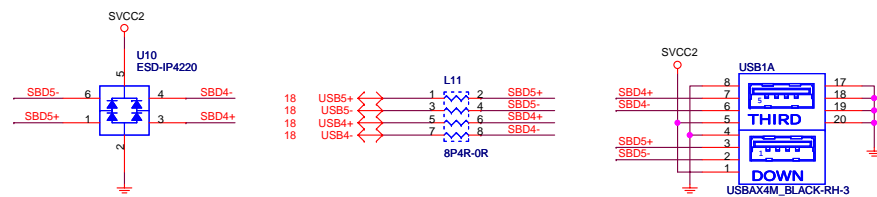


REAR PANEL USB CONNECTOR FOR USB PORT 0,1



NEAR USB CONNECTOR

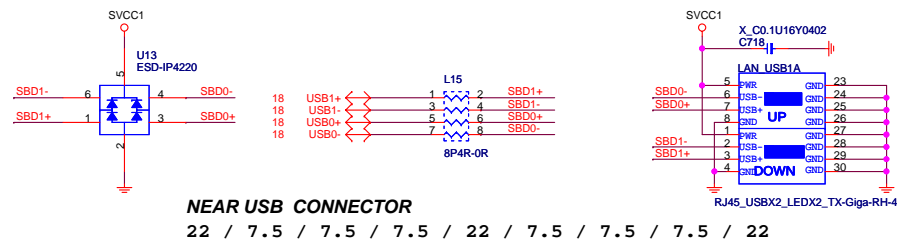
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22



NEAR USB CONNECTOR

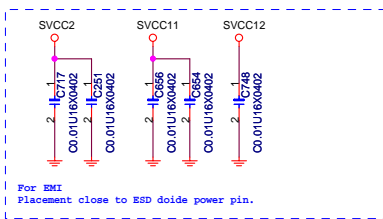
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REAR PANEL USB CONNECTOR FOR USB PORT 2,3



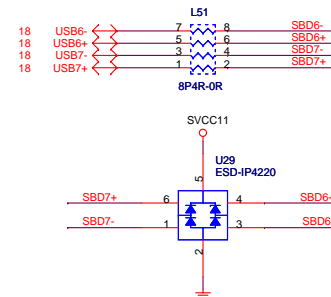
NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22



For EMI
Placement close to ESD diode power pin.

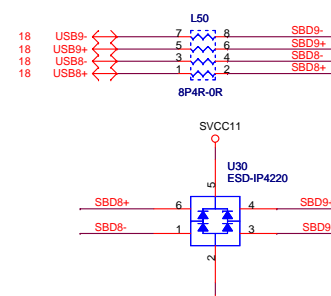
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

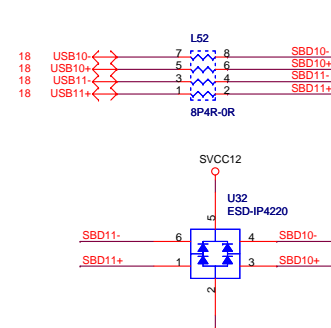
USB CARD READER + IR MODULE FOR USB PORT 8,9



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

USB CARD READER + IR MODULE FOR USB PORT 10,11

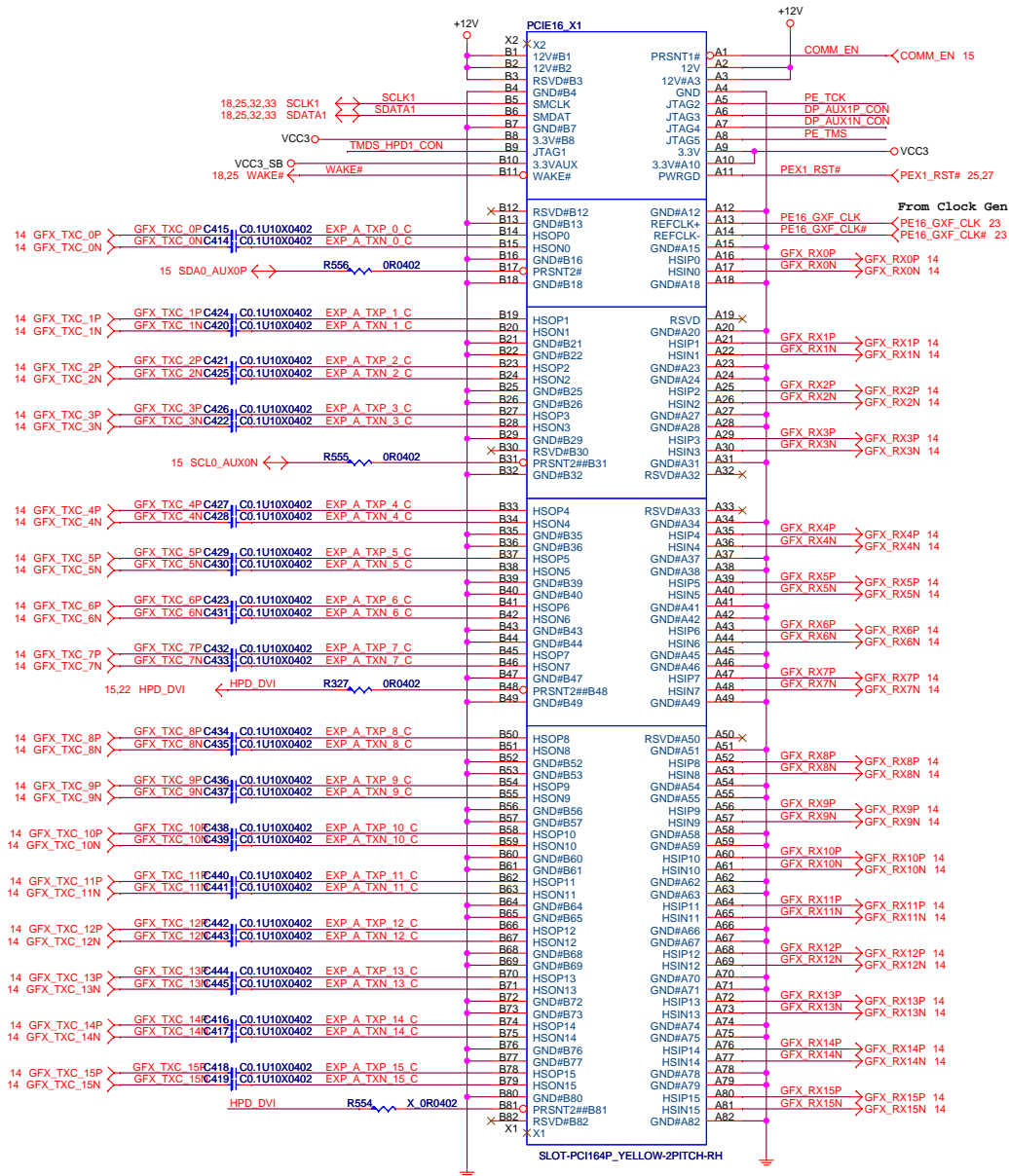


NEAR USB CONNECTOR

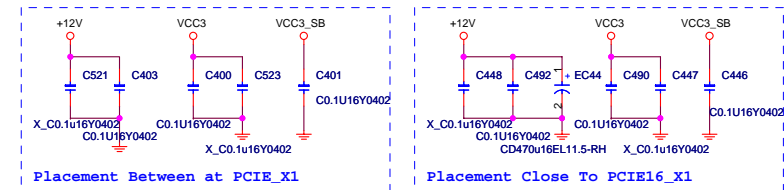
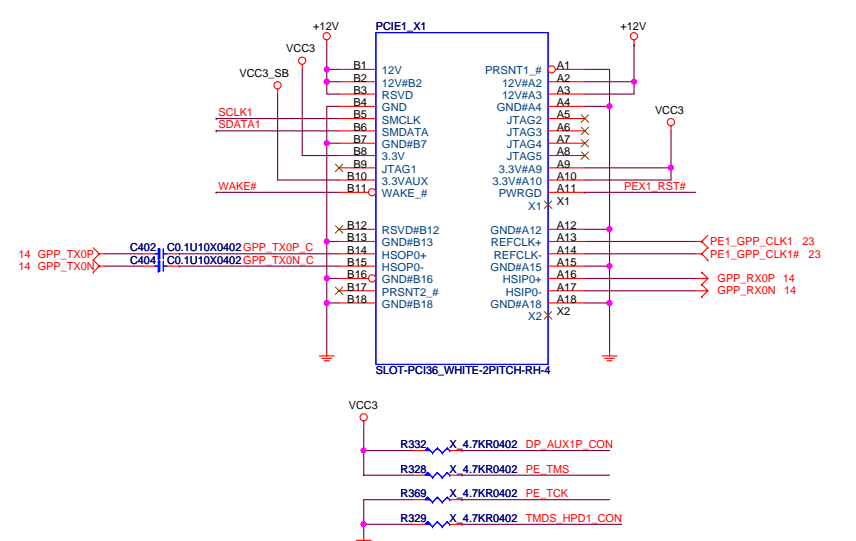
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

PCI Express Slot x16/x1

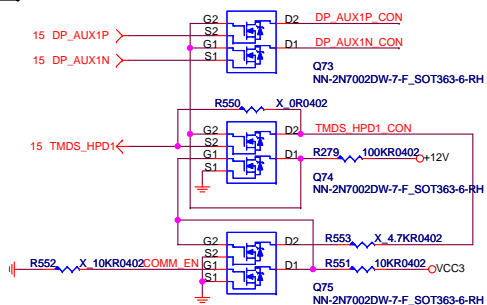
PCI EXPRESS x16 Slot

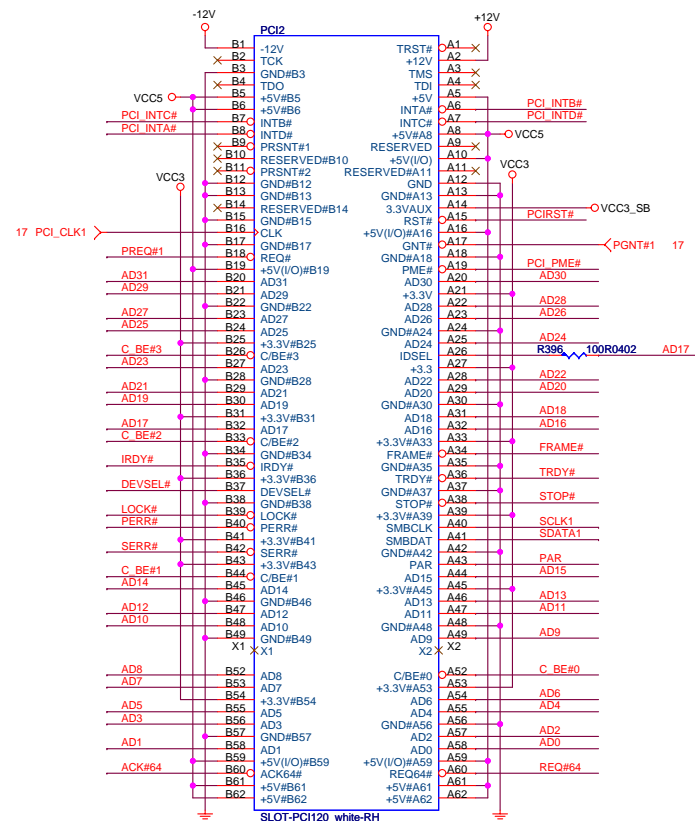


PCI EXPRESS 1 Slot-1



For Display Port

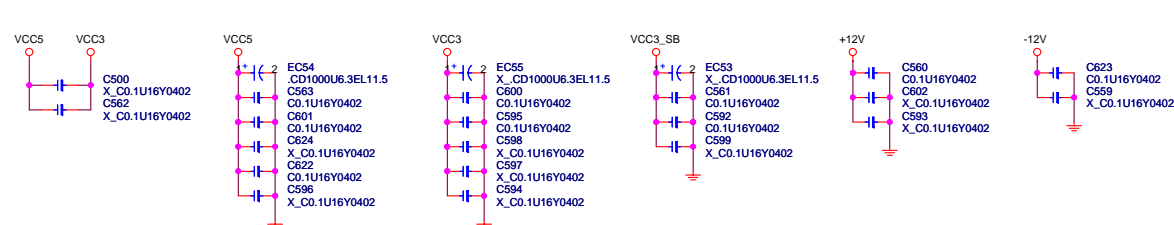


PCI SLOT 2 (PCI VER: 2.3 COMPLY)

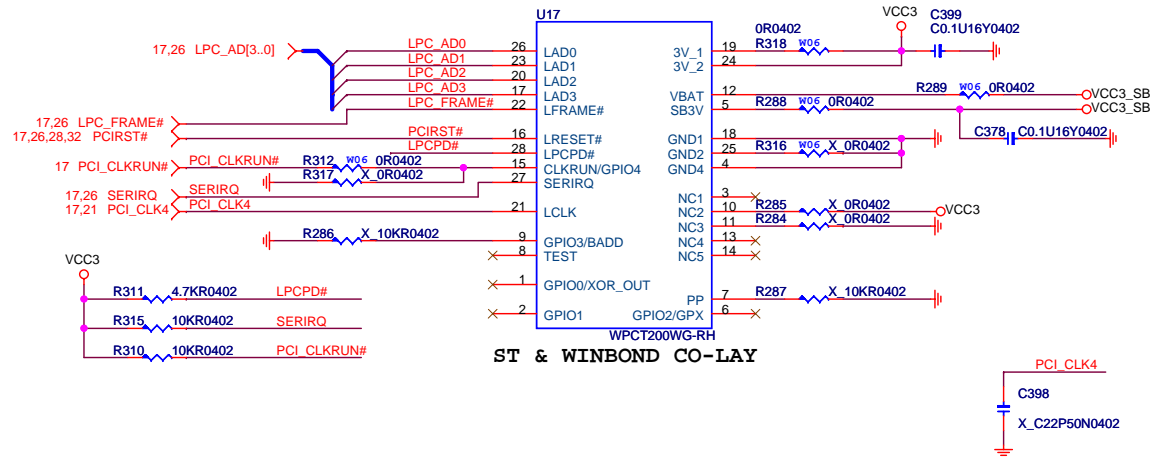
```
IDSEL = AD17
MASTER = PREQ#1
PCI INT B, C, D, A
```

17,28 AD[0..31] ← AD[0..31]
17,28 C_BE#[0..3] ← C_BE#[0..3]

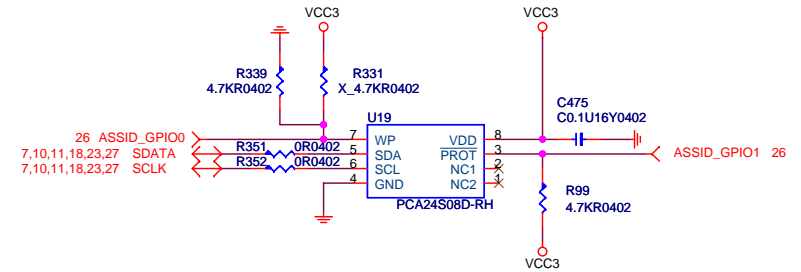
PCI SLOT DECOUPLING CAPACITORS



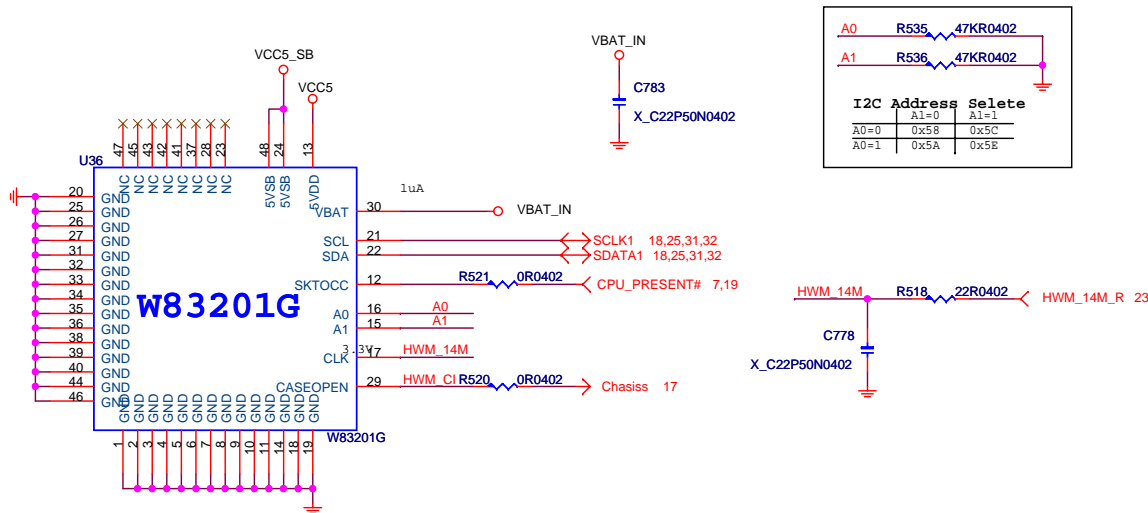
TPM Chipset



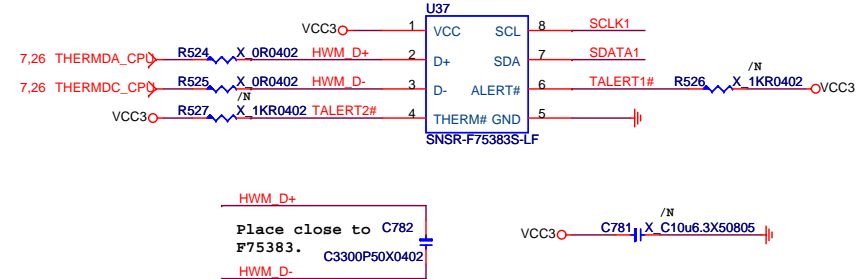
ASSET ID Chipset




ASF2.0 Hard Ware Monitor

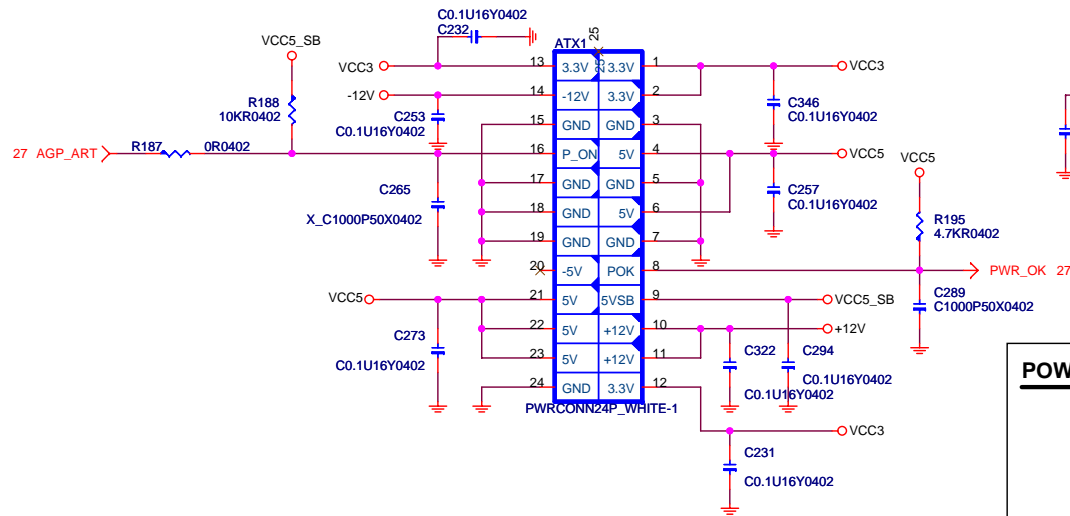


CPU Thermo Sense

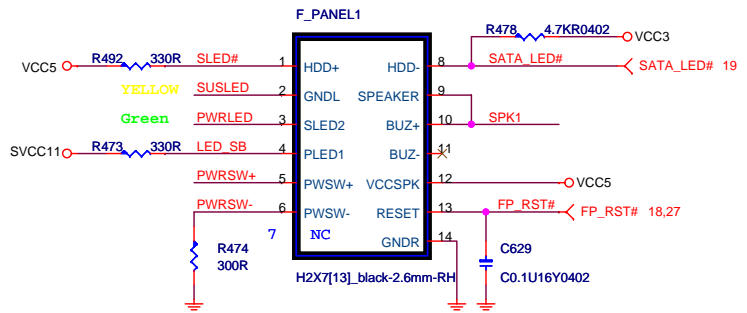


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Title TMP/Asset ID/HWM W83201G		
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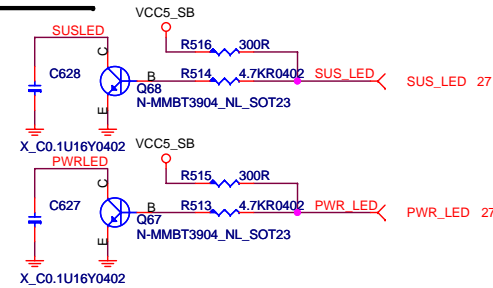
ATX CONNECTOR



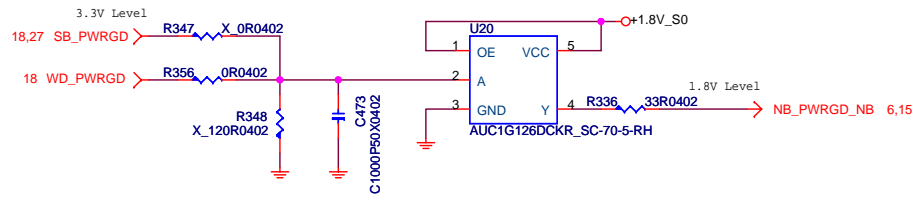
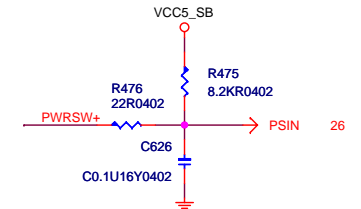
LENOVO Front Panel Connector



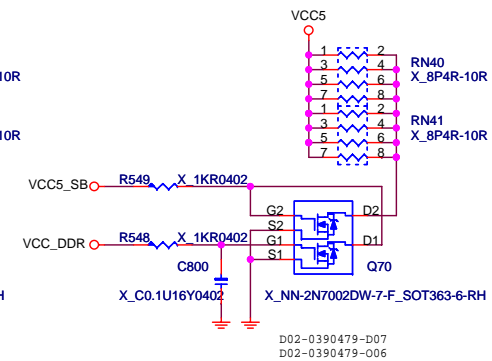
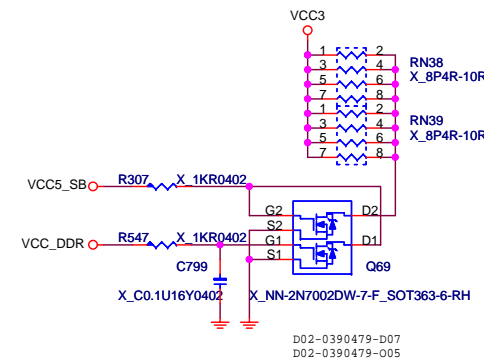
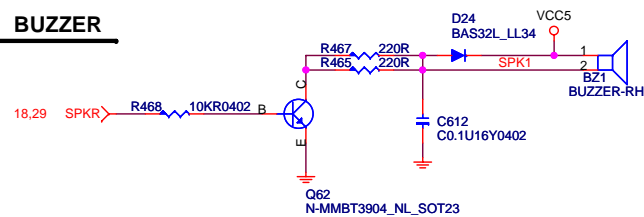
POWER LED




POWER BUTTON

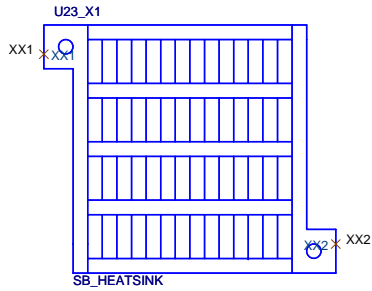
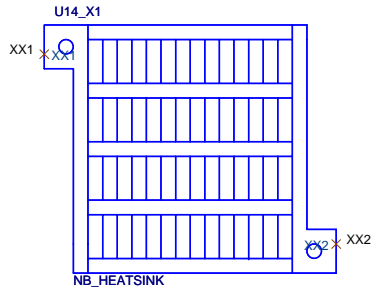


BUZZER



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ATX & FRONT PANEL		
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HEAT SINK

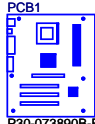


MANUAL PART



BAT1_X1
BAT-BCR2032P-RH

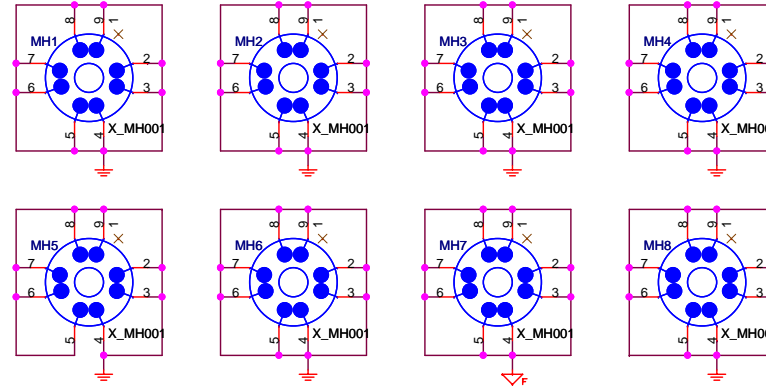
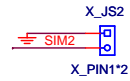
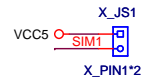
AVL:
D06-0100161-P52
D06-0100101-P01



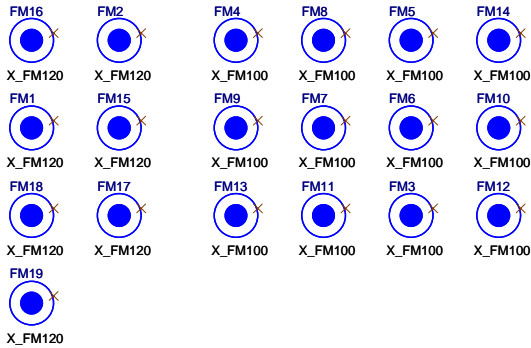
PCB1
P30-073890B-E48


P30-073890A-B48
P30-073890A-G37
P30-073890B-B48
P30-073890B-G37

Simulation



Optics Orientation Holes



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